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(54) Interfacing device for a computer games system.

(57) An interfacing device for connecting the processing unit of a computer games system to an external data storage medium has a user-operable selection unit for generating a user-selected address and user-selected data. The user-operable selection unit may comprise user-operable switches or electronic latches that are set by a program in response to selections made by the user by means of a joystick, keypad or any other input device. An address comparison unit compares the user-selected address with the addresses from the processing unit, and a data switching device causes the user-selected data to be substituted for data in the storage medium whenever the compared addresses are the same. Instead of a user-operable selection unit, preselected addresses and preselected data may be stored in a ROM, which in one embodiment changes the way the computer interprets external memory and in another changes the computer's internal memory itself.

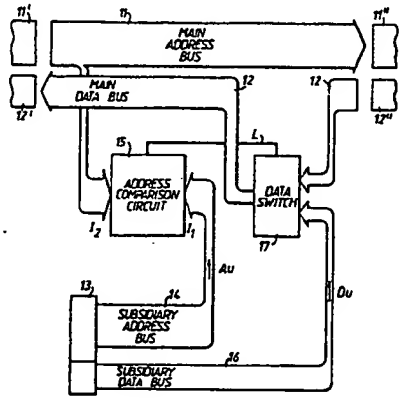

Fig.2.

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INTERFACING DEVICE FOR A COMPUTER GAMES SYSTEM

This invention relates to computer games systems and it relates particularly to an interfacing device for modifying the manner in which a computer game is played.

A conventional computer games system typically includes a computer containing the main processing unit, a visual display unit (VDU) on which a game is displayed and which may constitute a part of the computer, some form of interactive unit (e.g. a keyboard or a joystick), enabling a player or players to react to and influence events during the course of a game, and an external data storage medium (e.g. a cartridge) that can be plugged into or otherwise connected to the main processing unit and contains data defining the characteristics (e.g. the rules) of the particular game being played.

In general terms, the main processing unit is programmed to address different storage locations in the external data storage medium, whereby to access the stored data as it is needed.

To that end, the main processing unit generates an address identifying a respective storage location in the storage medium, and this address is routed to the storage medium on an address bus. When the stored data is required, the processing unit sends a request signal to the storage medium, whereupon the data in the addressed storage location is accessed, and then routed to the processing unit on a data bus.

The data stored in an external data storage medium determines the characteristics of the game stored therein and would typically define such game parameters as the number of playing units (e.g. cars, planes, etc.), the number of lives ascribed to individual players, the duration of particular events, time limits and speed settings, colour and so on.

Generally, computer games require the players to complete various tasks (e.g. to complete a fixed number of laps of a track), and failure to complete a task satisfactory results in some cases in the elimination of a player from the game. In many games, the players may be ascribed more than one "life" and this can affect the difficulty, or ease, with which the game is played,

With existing systems, the characteristics of a game, and in particular its degree of difficulty, are to a large extent predetermined by the data stored in the external data storage medium. Consequently, existing computer games tend to lose their appeal and present less of a challenge to the player the more times they are played that is to say the games have limited "playability".

It is an object of the present invention to alleviate the aforementioned shortcomings of existing computer games systems that use an external data storage medium such as a cartridge with a read-only memory (ROM) and the like.

Another object of the invention is to provide an interfacing device for connecting a processing unit of a computer games system to an external data storage medium, the interfacing device being capable of operating in various ways, either user-selected or preset, for modifying the rules of the game, thereby enhancing the playability of the game.

According to the invention there is provided an interfacing device for connecting the processing unit of a computer games system to an external data storage medium so as to enable the processing unit to address, and receive data from, different storage locations in the external data storage medium, the interfacing device comprising means responsive to the processing unit for recognition of a selected address and means for modification of data processed by the processing unit in response to said recognition.

With an interfacing device constructed in accordance with the invention, the user has the capability to substitute his own, user-generated data for that which would otherwise be supplied to the processing unit by the external data storage medium, and in this way the user can control and radically change the parameters of the game normally defined by the data stored in the external data storage medium and thereby enhance the "playability" of the game.

In a particular embodiment of the invention, the modifying means comprises user-operable means for generating a first signal and a second signal representing the selected address and user-selected data respectively, means for comparing the selected address represented by the first signal with an address from the processing unit, and means for supplying the user-selected data to the processing unit in substitution for the data in the addressed storage location of the external data storage medium if the compared addresses are the same.

The supplying means may be a semiconductor switching device responsive to an output from the comparing means.

In accordance with another aspect of the invention, there is provided a computer games system comprising a main processing unit, an external data storage medium and an interfacing device, in accordance with the first aspect of the invention, for interconnecting the main processing unit and the external data storage medium.

According to a yet further aspect of the invention, there is provided a method of playing a computer game using a computer games system having a processing unit and an external data storage medium, including the steps of comparing an address from the processing unit with a selected address and modifying data supplied to the processing unit whenever the compared addresses are the same.

In accordance with another aspect of the invention, the modifying of the data takes place only if the data from the external data storage medium matches data set by user-operable input means (which may be switches, keypad, joystick, etc.). In other words, the data is modified only if it is what the interface expects to find there. Some large programs have "bank switching", which means that several banks of data are stored at each address. This "data compare" feature of the invention ensures that only data at the correct address and the correct bank is modified.

Interfacing devices embodying the present invention are now described, by way of example only, with reference to the accompanying drawings, in which:-

Figures 1a, 1b and 1c are respectively top plan, side and perspective views of an interfacing device in accordance with the invention;

Figure 2 is a block diagram of circuitry used in the interfacing device of Figures 1a, 1b and 1c;

Figure 3 shows the circuitry of Figure 2 in more detail;

Figures 4a, 4b and 4c are respectively top plan, side and perspective views of another interfacing device in accordance with the invention;

Figure 5 is a block diagram of circuitry used in the interfacing device of Figure 4;

Figure 6 is a block diagram of an alternative embodiment of the invention;

Figures 7a, 7b and 7c are respectively top plan, side and perspective views of another embodiment of an interfacing device according to the invention;

Figure 7d is a perspective view showing an embodiment of the present invention just prior to its connection to a game cartridge;

Figure 7e is a perspective view showing apparatus in accordance with the invention after it has been connected with a game cartridge to form an assembly;

Figure 7f is a perspective view showing the assembly of Figure 7e just prior to insertion in a games machine;

Figure 7g is a side elevation showing the apparatus after the insertion of the assembly of Figure 7e in a games machine;

Figures 8a and 8b collectively form a block diagram of circuitry used in the interfacing device of Figures 7a, 7b and 7c;

Figure 8c is a more detailed block diagram of a portion of the circuitry of Figure 8a; and

Figure 9a shows a block circuit diagram of a graphics generating arrangement and Figures 9b and 9c represent graphics data generated by the arrangement of Figure 9a;

Figures 10a, 10b and 10c when taken together form a flow chart showing the operation of the circuitry of Figures 8a to 8c.

The interfacing device, shown generally in Figures 1a, 1b and 1c, comprises a shallow case 1 of which one end 2 is intended to fit into a receiving port of a computer games console such as the well-known Nintendo console and the opposite end 3 is intended to receive an external data storage medium (hereinafter referred to as an external memory), such as a cartridge having a read-only memory (ROM).

The case contains a printed circuit board 4 that carries interfacing circuitry, the board 4 being provided at each end thereof with suitable end connectors enabling the interfacing circuit to detachably interconnect the main processing unit of the games console and the external memory.

As will become clear hereinafter, in this embodiment of the invention user-adjustable switches 5, set into the upper wall 6 of case 1 may be utilised to modify the manner in which a game stored in the memory is played. In the illustrated example, six 16-position rotary switches are provided.

As Figure 2 shows, the interfacing circuitry comprises a main address bus 11 for interconnecting the address bus $11'$ of the main processing unit and the address bus $11''$ of the external memory, whereby addresses can pass from the main processing unit to the memory.

Similarly, the interfacing circuit has a main data bus 12 which interconnects the data bus $12'$ of the main processing unit and the data bus $12''$ of the external memory, whereby data can pass from the external memory to the main processing unit in response to received addresses, provided such data has not been blocked by circuitry (to be described) in the interfacing device.

The interfacing device has a user-operable selection unit 13 by which the user can generate a user-selectable address (A_u) and user-selectable data (D_u). The user-selectable address (A_u) is routed on a subsidiary address bus 14 to one input I_1 of an address comparison circuit 15, and the user-selectable data (D_u) is routed on a subsidiary data bus 16 to an input of a data switching device 17. As Figure 2 shows,

addresses on the main address bus 11 (which are, of course, generated in the main processing unit) are routed to a second input I_2 of the address comparison circuit 15 for comparison with the user-selectable address (A_u) at the first input I_1.

If the compared addresses are different, data from the memory is routed, via the switching device 17, onto the main data bus 12 for onward transmission to the main processing unit.

If, however, the compared addresses are the same, the address comparison circuit 15 generates an actuation signal on line L causing the data switching device 17 to change its switching condition, blocking the transmission of data from the external memory and routing the user-selected data D_u onto the main data bus 12 for onward transmission to the main processing unit.

By this means, the user-selected data generated by selection unit 13 is substituted for data from the respective storage location of the external memory upon recognition of an address selected by the user.

This substitution may be illustrated by the following simple example.

It will be assumed that the user has set the user-selectable address A_u at a value 1002 (which location contains "7") and the user-selectable data D_u at a value "3". In fact, as will be described hereinafter, the selected address and data are normally encoded in accordance with the hexadecimal coding format, though of course this is not a requirement.

If the current address from the processing unit is 1001, say, it would not be recognised by the address comparison circuit 15 and so the data held in the addressed storage location of the external memory (i.e. that corresponding to address 1001) is routed to the main processing unit on the main data bus 12. The stored data supplied to the processing unit in this way might have the value "9", say, different from the value of the user-selected data.

If, on the other hand, the current address from the processing unit is the same as that selected by the user, then the user-selected data, having the value "3", is supplied to the processing unit in substitution for the data stored in the addressed storage location of the external memory.

The alternative data values ("3" and "7") may represent the number of lives ascribed to a player and so, by changing the value from "7" (the value stored in the external memory) to a different value ("3" in this example), the user has the capability to modify (increase in this example) the difficulty of the game to a desired extent.

Figure 3 shows the interfacing circuit in somewhat more detail. The main address and data buses, which interconnect the main processing unit and the external memory, are again referenced at 11 and 12 respectively, and a data request bus is also shown at 18.

The user-controllable selection unit 13 comprises two banks 21,22 of user-selectable switches, one 21 of the banks comprising switches Ao.....A14, for setting the user-selectable address A_u, and the other 22 of the banks comprising switches Do.....D7 for setting the user-selectable data D_u.

The switching arrangement shown is appropriate to generate binary address and data signals encoded in accordance with the hexadecimal coding format and can in practice be embodied as respectively four and two 16-position rotary, or alternatively configured, switches. Alternatively, a pre-set plug-in pin connection package could be used instead of an arrangement of switches.

The user-selectable address and data signals could alternatively be held in latches. In this case many types of data entry system (e.g. keypad, voice input) can be used to set the latches.

The data switching device 17, comprises three identical integrated-circuit data switches 23(1), 23(2), 23-(3) (Ref.No. 74HC4053P) which are connected, as shown, to the external memory and to the bank of switches 22 by the main and subsidiary data buses 12 and 16, respectively.

The address comparison circuit 15 comprises two identical integrated circuits 24(1),24(2) (Ref. No: 74LS684N) that are connected, as shown, to the main processing unit and the bank of switches 21 by the main and subsidiary address buses 11,14 respectively, and an integrated OR gate 25 (Ref. No: 74LS32) is provided to effect a change in the switching condition of the device 17 in response to recognition by the address comparison circuit 15 of an address selected by the user.

While the described embodiment enables recognition of a single address and substitution of data corresponding thereto, the invention also embraces recognition of two or more different addresses and substitution of the respective data corresponding thereto.

In another embodiment of the invention, shown in Figures 4 and 5, the interfacing device utilises preselected addresses and preselected data.

The embodiment shown in Figures 4 and 5 is similar to that shown in Figures 1 to 3, and common components are given like reference numerals.

However, in this embodiment, the user operable switch (shown at 13 Figures 2 and 3) is replaced by an internal memory in the form of a read only memory (ROM) 40.

The subsidiary address bus 14 connects the address output of the ROM 40 to a 24-bit address

comparison circuit 15 via two address latches 41 and 42 that are connected in parallel, and the subsidiary data bus 16 connects the data output from the ROM 40 to the input of an 8-bit buffer 43 via a further latch 44. The output of buffer 43 is connected to the main data bus 12, which, as shown, also incorporates an 8-bit buffer 45.

Both buffers 43 and 45 are controlled by an address comparison signal L generated by the address comparison circuit 15, whereby data is selectively routed to the processing unit either on the main data bus 12 or on the subsidiary data bus 16, depending on the result of a comparison carried out in the address comparison circuit.

Latches 41 and 42 are set to hold the high and low bytes respectively of a preselected, two-byte (16-bit) address A_p transmitted thereto from ROM 40 over the subsidiary address bus 14.

Similarly, the latch 44 is set to hold pre-selected data D_p (corresponding to the preselected address A_p in latches 41 and 42) transmitted thereto from the ROM 40 over the subsidiary data bus 16.

The preselected address A_p held in latches 41 and 42 is compared with current addresses transmitted from the processing unit over the main address bus 11.

If the compared addresses are different, the address comparison signal L goes high, thereby maintaining buffer 43 (which is supplied via an inverter 43a) closed and buffer 45 (which is supplied via a logical AND gate 46) open and allowing data to pass directly from the external memory to the processing unit over the main data bus 12.

However, if the compared addresses are the same, the address comparison signal L goes low, thereby maintaining buffer 43 open and buffer 45 closed and enabling the preselected data D_p held in latch 44 to pass to the processing unit in substitution for the data in the external memory.

In this embodiment, the interfacing device has the capability to modify data received from any one of a range of different external data storage media (containing different computer games) that can be plugged into the device.

To that end, the ROM 40 stores a plurality of different preselected addresses together with a corresponding plurality of different preselected data, and each preselected address is utilised in conjunction with the corresponding preselected data to modify the data from a respective external memory.

Clearly, in order to access the correct preselected address (and data) to the latches, to enable address comparison and (possible) data substitution to take place, the interfacing device must be capable of identifying which external memory has been plugged into its receiving port.

To that end, additional control circuitry is provided that, in effect, enables the interfacing device to interrogate two data bytes of the external memory.

These data bytes carry sufficient information to unambiguously identify the external memory and thereby enable the correct preselected address and the corresponding preselected data, to be accessed to latches 41, 42 and 44 to facilitate the desired data substitution, as described hereinbefore.

The identification procedure is controlled by means of a controller 50 which is clocked by a counter 51 operating in conjunction with a clock circuit 52 and a "power-on" timing circuit 53.

When the external memory is first plugged into the interfacing device and power is supplied to the processing unit, the counter 51 is initialised and the external memory is isolated from the processing unit (by setting input A of the AND gate 46 low).

The controller 50 then transmits successive control signals to the ROM 40 on a control bus 54, causing the high and low bytes of the first address stored in the ROM 40 (corresponding to the first data byte for identification in the external memory) to be routed to latches 55 and 56 respectively. In this way, latches 55 and 56, which are connected to the external memory via the main address bus 12, are set to hold the first address (corresponding to the first data byte in the external memory). In response to this address, the first data byte is transferred from the external memory to an encoder 57 (the main data bus 12 being blocked by buffer 46), where it is latched. This procedure is repeated for the second data byte for identification in the external memory, which is also transferred to, and latched in, the encoder 57.

The encoder 57 then performs preset, logical operations on the first and second latched data bytes and generates an output that uniquely identifies the external memory. This output is held in a ROM latch 58 (which had previously held a zero data field), and the encoder 57 is then disabled. The controller 57 selects from the ROM 40 the pre-selected address (and the preselected data) appropriate for the external memory represented by the output held in ROM latch 58 and causes the high and low bytes of this preselected address to be transferred to latches 41 and 42 respectively and the required preselected data to be transferred to latch 44.

As described hereinbefore, the address comparison circuit 15 compares the latched, preselected address with the current addresses from the processing unit. However, the address comparison circuit 15 also compares current data transmitted from the external memory over the main data bus with data held in

a fourth latch 47. The latched data (which is also derived from ROM 40) is chosen to be the same as the data (from the external memory) which is to be replaced by the preselected data held in latch 44. This additional comparison ensures substitution of the correct data and prevents errors which could arise as a result of an ambiguity in the process of comparing addresses.

The ROM 40 may have a number of different data banks, and so the data and address associated with each external memory may have a number of alternative values. In these circumstances, a user-operable switch 59 may be provided, enabling the user to select a desired data bank from the ROM 40 and thereby select a desired effect, e.g. a desired degree of difficulty (hard, medium or easy, say) with which the game is to be played.

In the described embodiment, each preselected address is allocated to a respective external memory. Alternatively, however, more than one of the preselected addresses could be allocated to the same external memory, thereby enabling more than one aspect of a game to be changed.

In another embodiment of the invention, illustrated in Figure 6, an interfacing device for a computer games machine connects to the external program cartridge, and the computer games machine allows the program cartridge to function normally except for one or more modifications performed by the interface.

These modifications affect one or more aspects of the game and can be either user-selectable or preset in the interface.

In this respect, the embodiment of Figure 6 is the same as the other embodiments.

However, in the embodiment of Figure 6, the interface allows the program to execute normally but interrupts the processor at a particular point or points (user-selectable or preset) in the program. When this interrupt occurs, the game is temporarily suspended while the interface banks its own ROM into the processor's memory and executes a piece of code. This code is such that a modification is effected on the games computer's internal memory. This interface then banks its own ROM out and allows the computer to continue executing the game as if nothing had happened.

This process allows a user or a preset ROM to change many of the variables that control aspects of a game, modifying the game in countless different ways.

The effect of this is very similar to the effect of the previous embodiments. The manner of operation is, however, different. Instead of changing the way the computer interprets or accesses external memory, this method changes the computer's internal memory itself in such a way that very similar results can be achieved: e.g., extra lives, skipped levels, increased or decreased car speed etc.

Conventional devices that interrupt a program perform a designated function and then pass control back to original program. The purpose is normally to perform additional tasks rather than to change the way the existing program works. Also, the conventional devices are normally "stand-alone units" that do the same thing regardless of the program that is running. In contrast, the apparatus of the present invention produces its visible and audible effects in a manner that is intrinsically dependent on the "host" program. Moreover, it acts as an interface between the computer and the external memory in order to prevent access to the external memory when it wants to present its own program to the computer instead.

Conventional interrupt-controlled devices are activated entirely independently of the program that is running. In contrast, apparatus constructed in accordance with the present invention is activated upon detection of the exact address of a particular piece of program being accessed. It then makes changes to the computer's internal memory to affect the way the program works. This is not needed in conventional usage because it is easier for the original programmer to make the change before the external memory is produced.

In Figure 6, the device 70 is an interface between a games computer (via edge connector 71) and a plug-in game cartridge external memory (via edge connector 72).

The address comparator circuit 73 compares the value of the address bus 74 with a preset value, in this case a value supplied on a bus 75 from registers 1 and 2.

When the compared values are different (i.e. normally), the computer accesses the external memory unhindered.

When the compared values are equal (i.e. the program is at the correct stage for the device to interrupt), an output signal is sent on control line A to a switch circuit 76, which in a practical embodiment may be a semiconductor device.

This has the effect of connecting the output enable line 80 from the computer through the switch 76 and alternative output enable line 81 to the device's internal ROM 77 instead of connecting the output enable line 80 to the external memory edge connector 72 through the extension 80a. At this point the computer starts addressing the ROM 77 instead of the external memory.

The ROM 77 can then make changes to the RAM and other registers housed in the computer (or in the interface 70) to effect changes in the way the program operates.

The switch 76 then reverses and re-enables the external memory by switching the output enable line 80 back to connect from the computer to the external memory through the extension 80a. In this example this is done by way of register 3, which controls control line B.

The program then continues where it left off but operating differently because of the changes that have been made.

When the external memory programs (games) are running on a computer, they constantly use the computer's internal RAM as a temporary scratch-pad for storing values that change. These values are typically used for parameters such as number of lives remaining, current level number, counters for timing loops (speed), number of cars, etc. In accordance with the present invention, the user - or the programmer of the ROM 77 - can change these values in response to reaching a particular point in the program.

Figures 7a, 7b and 7c are respectively top plan, side and perspective views of another embodiment of an interfacing device according to the invention. These Figures show the best mode contemplated by the inventors for putting the invention into practice. The device comprises, as in the embodiments described above, a case 1 of which one end 2 is intended to fit within a receiving port of a computer games console and the opposite end 3 is intended to receive an external data storage medium or memory, such as a cartridge having a read-only memory or ROM.

The case contains, as in the embodiments described above, a printed circuit board 4 that carries interfacing circuitry, the board 4 being provided at each end thereof with suitable end connectors enabling the interfacing circuit to detachably interconnect the main processing unit of the games console and the external memory.

A handle portion H of generally triangular construction (as viewed from above) has a concave thumb rest TR provided with ridges R. The external data storage medium is connectable to the interfacing device in such a manner as to be positioned underneath the handle portion H. By virtue of the concave thumb rest TR formed on the upper surface of the handle portion H, an assembly of the interfacing device and the external data storage medium can conveniently be grasped with a thumb engaging the thumb rest TR and fingers engaging the external data storage medium for connection of the assembly to the processing unit of a computer games system.

Figure 7d is a perspective view showing a "game X", which can be any conventional game cartridge, about to be assembled with the device according to the invention. Figure 7e shows the game cartridge and the device according to the invention in assembled relation, and Figure 7f shows the assembly about to be inserted into a games machine, for example a Nintendo machine. As noted above, the assembly is conveniently grasped with the thumb of the user in the thumb rest TR and the fingers of the user below the game cartridge. The assembly is inserted and appears then as in Figure 7g, with the lid of the games machine resting on the thumb rest TR. The thumb grip prevents the game cartridge from being inserted upside down, partly because of its physical size and partly by a notch N which would catch against the lower edge of the entry port of the games machine.

The printed circuit board 4 is thicker than normal, to allow the edge connector to make good contact (by a wedging effect) with the games machine connector without the need for the interface to be pushed down fully in the normal way. In this way, connection of the interface to the processing unit can be effected by a rectilinear movement. This enables the unit to be made smaller and more elegant.

The circuitry incorporated in the device of Figures 7a to 7g is illustrated in Figures 8a to 8c. The circuitry shown in these Figures has two modes of operation. Mode 1 is a latch-setting mode, wherein values for the address comparison, data comparison, and data replacement functions are set by the user. Mode 2 is an active mode, very similar to the operation of the embodiments described above, wherein the address comparators (as well as data comparators) send a signal to a data.replacement unit to effect a replacement of the data when the conditions for data replacement are met.

The selection of modes is made over line 102 from the control latch 103. A CE line 92 that comes from the computer edge connector 71 is connected to the CE selector 90 which is controlled by line 102. In conventional structures, the line 92 would normally connect directly to the external memory, allowing it to respond to data read/write requests from the video games machine. In the circuit of Figure 8a, the signal on the line 92 is passed either to the external memory 93 via a CE' line 94 or to an interface ROM 96 via a CE'' line 98 depending on the state of line 102. In this way, either the external memory 93 or the interface ROM 98 is made active. The circuitry also has a power-on circuit 100, which ensures that the line 102 from the control latch is set to the latch setting mode when the power is first turned on.

MODE I: LATCH-SETTING MODE

The purpose of this mode is to allow the user to select the address comparison data and replacement data. The program in the ROM 96 is designed in such a way that it will accept input from the normal game control pad, operated by the user, and use it to move an on-screen pointer around the screen. Also, on the screen there are 16 different letters (which represent values). The user can move the pointer to any of these letters and select them using a button on the game control pad. By repeating this process the user can enter this data to represent addresses, comparison data bytes and replacement data bytes, as well as function enable/disable information. When the user presses the start button on the game controller, the software stores the data entered by the user in the latches in each of the comparison/replacement units 1, 2 and 3 as well as in a control latch 103.

It then sets bit O in the control latch 103 which alters the state of the mode select line 102 thereby switching the device to the active mode by changing the state of the CE selector 90 to its other position, conditionally enabling replacement units 1, 2 and 3.

MODE II: ACTIVE MODE

In this mode, the external memory has control of the CPU and the game will function normally, with the exception of any data replacement operations performed by the interface. The comparison/replacement units are now active, provided that the appropriate bit in the control latch has been set to enable them.

The structure illustrated in Figures 8a, 8b and 8c includes an address bus 104 connected to comparison/replacement units 1, 2 and 3 and a data bus 105 connected to the same units. At the left of Figure 8a, the address and data buses connect to the games machine, and at the right to the game cartridge that is currently in use. In addition, a read/write line 106 is connected to the comparison/replacement units 1, 2 and 3, to the ROM 96 and to the video games machine and the particular game cartridge in use. The chip enable line 92 is connected to the chip enable or CE selector 90 as described before and also the comparison/replacement units 1, 2 and 3.

The address and data buses 104,105 are also connected to the ROM 96, and the address bus 104 is connected to a register address decoder 107. The latter produces four outputs which go respectively to inputs R.SEL O....3 of each of the comaprison/replacement units 1, 2 and 3. As Figure 8c shows, the latter input goes to a replacement data latch 0-7, a comparison data latch 0-7, a comparison address latch 0-7, and a comparison address latch 8-14.

The data bus 105 also connects to the control latch 103, which produces the output on the line 102 to the CE selector, as noted above. The output on the line 102 also goes to the register address decoder 107 and to an output to Figure 8b labelled G.CONT (graphics control).

The control latch 103 produces an output to an input labelled R.EN on each of the comparison/replacement units 1, 2 and 3 and an output to an input labelled DC.EN on each of the comparison/replacement units 1, 2 and 3.

Each of the comparison/replacement units 1, 2 and 3 produces an output on a terminal labelled REP ("replace") which is supplied to the CE selector 90.

In Figure 8b, the graphics address 0-12 bus is connected to a graphics generator 110, which produces an output to a graphic output buffer 111. A device selector 112 receives inputs from the G.CONT terminal and from a G CE terminal and produces outputs to the graphic output buffer 111 and the G CE terminal of the game cartridge. The graphics line G WE and G OE connect through Figure 8b from the games machine to the game cartridge in use.

In Figure 8c, the replacement data latch 0-7 connects to an 8 bit buffer 115. An 8-bit comparator 116 receives comparison inputs from the data line DO-7 and the comparison data latch 0-7 and produces an output signal to a control 117 when the inputs are equal. A fifteen bit comparator 118 receives at one input an output from the comparison address latch 0-7 and an output from the comparison address latch 8-14 and at the other input data from the address line 0-14. It produces a control output to the control 117 when the inputs are equal. The control 117 also receives signals from the R.EN, Read/Write, chip enable, DC.EN and F.EN terminals. Its output controls the 8-bit buffer 115 and is also fed to the output terminal REP.

The graphics generator 110 and the graphics output buffer 111 are shown in greater detail in Figure 9a.

A conventional graphics generator usually generates its screen display using data read out from a graphics ROM. This data defines the bit patterns that form the characters/shapes to be displayed on the screen. The screen is divided up into a plurality of character-sized areas (squares or rectangles) - character cells - each 8x8 pixels in size. Each such pixel is defined by two bits in memory, representing one of four colours and the graphics ROM usually has a minimum size of 8k bytes giving 512 different character cell definitions, as would be needed for a normal game. This memory size enables the system to generate

detailed, colourful and varied displays.

In the aforementioned latch-setting mode, the interfacing device uses the screen for display purposes, but only to a limited extent i.e. to display sixteen letters from which the player can make a selection to set user-selectable addresses and data, and various other letters. Accordingly, the graphics generator 110 does not need to have the storage capability of a conventional graphics generator.

Referring to Figure 9a, the graphics generator 110 comprises a logic circuit which, in effect, emulates a graphics ROM containing sixteen different character cell definitions, as represented in Figure 9b.

Even though the graphics produced with this system are cruder (only each group of 4 by 4 pixels is selectable on or off, instead of each pixel being individually selectable) it is perfectly acceptable for the required purposes.

In Figure 9a, a small logic circuit is added to the circuitry needed for the rest of the device. The circuit of Figure 9a has a negligible cost and size, in contrast to the substantial cost and size of the separate ROM which would otherwise be required.

The graphics generator and the graphics output buffer of Figure 9a together function as a graphics ROM emulator circuit.

In Figure 9a, the graphics generator 110 and graphics buffer output 111 are of course the same as the units shown schematically in Figure 8b. Figure 9a shows the inputs to the graphics generator 110 on lines GA 2, GA 4, GA 5, GA 6 and GA 7 and outputs on lines GD 0, GD 1, GD 2, GD 3, GD 4, GD 5, GD 6 and GD 7 plus a select input G. OE and C.CE′.

The graphics generator 110 includes four AND gates A1,A2,A3,A4, two OR gates 01,02 and an invertor I. If the input GA 2 is high, the OR gate 01 is high only if the input GA 4 is high and the OR gate 02 is high only if the input GA 5 is high. On the other hand, if GA 2 is low, then the OR gate 01 is high only if GA 6 is high and the OR gate 02 is high only if GA 7 is high.

The object of the circuitry in Figure 9a is to produce the 16 character bit patterns represented in Figure 9b, these patterns being numbered respectively 0-15. Since 4 x 4 pixels are addressed as a unit, there is a sacrifice of resolution, as indicated above, but, for reasons also indicated above, it is of no particular consequence. In Figure 9b (and also in the output portion of Figure 9c), a space that is not blackened corresponds to "0", and a space that is blackened corresponds to "1".

Figure 9c is a truth table showing the address lines in a logical order and the data values they produce to generate the 16 character cell definitions.

The operation of the circuitry of Figures 8 and 9 will now be described in connection with the flow chart of Figure 10.

Figures 10a, 10b and 10c when taken together form a flowchart showing the operation of the circuitry of Figures 8 and 9. When power is turned on as indicated at step 201 in Figure 10a, the process moves to step 202, wherein the control latch defaults to a value which sets the CE selector 90 so as to enable the ROM 96 on line CE″ 98. The process then moves to step 203, wherein the ROM 96 begins execution and the screen in accordance with the invention appears on the display screen on which the game is displayed.

At step 204, the program in the ROM determines whether the user has pressed a button on the control pad. If the user has not pressed such a button, the program loops back and makes the determination repeatedly until it is found that the user has pressed a button on the control pad. When the affirmative determination is made, the program moves to step 205, wherein a determination is made whether a movement button has been pressed by the user. If so, then at step 206 the program moves the cursor to a new letter and then reverts to step 204. If no movement button has been pressed, the program determines whether a fire button has been pressed by the user. If so, the program causes display of the letter under the cursor on the screen as a selected letter and then loops back to step 204. If the fire button is not found to have been pressed, the program determines at step 209 whether the start button has been pressed. If not, the program loops back to step 204.

When the start button has been pressed, then, as Figure 10b shows, the program converts the selected letters (if any) to hexadecimal values which represent data to be stored in the latches. At step 211, the program then stores hexadecimal values in latches corresponding to the addresses, data replacement values, and data compare values (if any). Then, at step 212, a program is transferred to the control deck's internal RAM. At step 213, control is passed to the program in the RAM.

At step 214, the program internal memory stores a value in the control latch with the CE selector bit set so as to enable the external memory on the line CE′ 94 (Figure 8a) and conditionally enable the replacement units and disable graphic emulation. At step 215, control is passed to the reset address of the external memory and, at step 216, the game program begins execution.

At step 217, the device determines whether the game control is requesting a read from the external memory. If not, it loops back until an affirmative determination is made. When an affirmative determination

is made, the device determines whether the value of the address bus corresponds to the address stored in one of the comparison/replacement units 1, 2 and 3. If not, the process loops back to step 217. When an affirmative determination is made, the process advances to step 219 (Figure 10c).

At step 219, a determination is made whether the corresponding comparison/replacement function is enabled. If not, the process loops back to step 217. When it is found at step 219 that the corresponding comparison/ replacement function is enabled, then, at step 220, a determination is made whether the corresponding data comparison function is enabled. If it is determined that the function has been enabled, the process advances to step 221, where a determination is made whether the value of the data bus corresponds to the comparison data stored in the corresponding address/comparison unit. If no such correspondence is found, the process loops back to step 217.

If at step 220 the corresponding data comparison function is not enabled, or if at step 221 the value of the data bus is found to correspond to the comparison data stored in the corresponding data/comparison latch, the process moves to step 222. At step 222, the external memory is prevented from outputting data by setting the CE selector to disable the line CE' 94 (Figure 8a) via the terminal Ref. Then, at step 223, the corresponding comparison/replacement unit is set to output the data stored in its data replacement latch to the data bus.

At step 225, a determination is made whether the read cycle is finished. If not, the process stays in the loop at step 225 until it is determined that the read cycle is finished. When the read cycle is finished, the process advances to step 226. At step 226, the corresponding comparison/replacement unit is prevented from outputting data. Then, at step 227, the external memory is re-enabled by enabling the line CE' 94 (Figure 8a). The process then loops back to step 217 in Figure 10b.

The versatility of the described interfacing devices is demonstrated by short extracts from typical computer games programs given in Examples I and II below.

In these Examples, the four-digit numbers (e.g. 3000) appearing in the left-hand column are coded addresses; they are followed by coded instructions (e.g. DEC1000) from the addressed storage location of the external memory. In fact, in the Examples given, each instruction consists of two or three bytes. An explanation of the function of each instruction is given in the right-hand column.

EXAMPLE I

This section of program causes a playing unit, e.g. a plane or car, to move at a particular speed.

ADDRESS	INSTRUCTION	EXPLANATION
3000	DEC 1000	This reduces the content of address 1000 by 1 (e.g. a value 28 changes to 27)
3003	BNE 300D	If the value of the last step is not zero the program returns to address 3000
3005	LDA 50	This puts value 50 (from the storage location corresponding to address 3006) into a variable "A".
3007	STA 1000	This puts the value of variable A (i.e. 50) into address 1000.
300A	JSR "MOVE UNIT"	Calls up subroutine "MOVE UNIT" which causes the unit to move.
300D	JMP 3000	The section of the program set out above is repeated

This section of programme causes the subroutine "MOVE UNIT" to be executed when the program steps corresponding to addresses 3000 to 3003 have been executed 50 times.

If, therefore, the interfacing device sets the selected address at 3006, and sets the selected data value at 10, then the value 50, in variable "A" in the processor, (the value in the corresponding storage location of the memory) is replaced by the user-selected value (10 in this example). This would cause sub-routine "MOVE UNIT" to be executed when the program steps corresponding to addresses 3000 to 3003 have been executed 10 times instead of 50 times.

Consequently the playing unit would be caused to move more quickly.

EXAMPLE II

In this game, a player is required to complete a given number of laps of a track.

ADDRESS	INSTRUCTION	EXPLANATION
2000	INC 1200 (LAP COUNT)	This increments the content of address 1200 by one (increasing the lap count by one every time a player completes a lap.)
2002	LDA 1200	This puts the content of address 1200 into variable A (i.e. it puts the current lap count into variable "A")
2004	CMP 3 (LAP 3?)	This compares the last value of the lap count with 3 (the value derived from the storage location corresponding to address 2005)
2006	BNE 200A	If the answer is no (i.e. the comparison shows an inequality), then the program goes to 200A; otherwise it continues on.
2008	JMP "RACE COMPLETE"	This causes a jump to the "RACE COMPLETE" part of the program.

The number of laps required to be completed by the player is set at the value 3 derived from the addressed storage location of the memory. If, therefore, the interfacing device sets the selected address at 2005, and sets the selected data value at 7, say, then the value 3 in variable A in the processor (the value derived from the memory) is replaced by the selected value, 7 in this example.

This requires the player to complete 7 instead of 3 laps, thereby increasing the difficulty of the game.

Clearly, these examples are merely illustrative of the many different modifications which could be effected using the interfacing device of the invention. The examples given effect a change of a single byte in a data table so as to change selected game variables such as screen colour, sound volume, number of players, number of laps, time intervals etc.

However, changes could alternatively, or additionally, be made to the instructions themselves; e.g. to change an instruction to increase a value to an instruction, to decrease a value, to change an instruction to perform a particular task to one which requires no action, to change a branch instruction. (BEQ to BNE, say) and so on.

Although the described embodiments enable recognition of a single address and substitution of data corresponding thereto, the invention also embraces recognition of two or more different addresses and substitution of the respective data corresponding thereto.

Also, although the specific embodiments relate to a detachable interfacing device, the device can alternatively be incorporated into the processing unit as an integral part thereof.

Claims

1. An interfacing device for connecting a processing unit of a computer games system to an external data storage medium so as to enable the processing unit to address, and receive data from, different storage locations in the external data storage medium, said interfacing device comprising means responsive to the processing unit for recognition of a selected address and means for modification of data processed by the processing unit in response to said recognition.

2. An interfacing device as claimed in claim 1, wherein said recognition means includes means for comparing the selected address with an address from the processing unit and said modification means effects the modification if the compared addresses are the same.

3. An interfacing device as claimed in claim 1 or claim 2, wherein the selected address is either an address selected by the user or a preselected address.

4. An interfacing device as claimed in claim 3, wherein the selected address is an address selected by the user and the modification means comprises user-operable selection means for generating a first signal and a second signal representing the selected address and user-selected data respectively, means for comparing the selected address represented by the first signal with an address from the processing unit, and means for supplying the user-selected data to the processing unit, in substitution for the data in the addressed storage location of the external data storage medium, if the compared addresses are the same.

5. An interfacing device as claimed in claim 4, wherein the data supplying means is a semiconductor switching device responsive to an output from the comparing means.

6. An interfacing device as claimed in claim 4, wherein the user-operable selection means comprises a first plurality of user-operable switching devices for setting the selected address and a second plurality of user-operable switching devices for setting the user-selected data.

7. An interfacing device as claimed in claim 6, wherein the switching devices are user-operable rotary switches.

8. An interfacing device according to claim 7, wherein the rotary switches are 16-position rotary switches.

9. An interfacing device according to claim 6, wherein the first plurality is four and the second plurality is two.

10. An interfacing device as claimed in claim 1, wherein the modification means comprises means for generating a first signal representing a selected address, a second signal representing data stored at said selected address in the external data storage medium, and a third signal representing selected data, means for comparing the selected address represented by the first signal with an address from the processing unit, means for comparing the data represented by the second signal with actual data at the selected address and means for supplying the selected data represented by the third signal to the processing unit, in substitution for the actual data, if both the compared addresses and the compared data are the same.

11. An interfacing device as claimed in any one of claims 1 to 10, wherein the modification means effects the modification in response to recognition of an address derived from a plurality of preselected addresses in dependence on identification data from the external data storage medium.

12. An interfacing device as claimed in claim 11, wherein the recognition means includes a memory for storing said plurality of preselected addresses together with a corresponding plurality of preselected data, and means for comparing said derived address with an address from the processing unit, and said modification means includes means for supplying to the processing unit the preselected data, corresponding to the derived address, in substitution for the data in the address storage location of the external data storage medium, if the compared addresses are the same.

13. An interfacing device as claimed in claim 12, wherein the preselected data, corresponding to one or more of said preselected addresses, has more than one user-selectable value, and including user-operable means to select one of the user-selectable values.

14. An interfacing device according to claim 1, wherein the modification means effects a modification in response to recognition of any one of two or more selected addresses from the processing unit.

15. An interfacing device as claimed in claim 1, wherein the modification means comprises a read-only memory, the processing unit includes an internal memory, and the modification means interrupts the processing unit in response to said recognition and banks data from said read-only memory into said processing unit in order to modify said internal memory.

16. An interfacing device as claimed in claim 15, wherein said address is either user-selected or is preset in said recognition means.

17. An interfacing device as claimed in claim 15 or claim 16, wherein said recognition means comprises bus means connected to said processing unit, register means, and comparator means connected to said bus means and said register means, said register means being adapted to store a value corresponding to said selected address and said comparator means producing an output indicative of correspondence between an address on said bus means and said stored value.

18. An interfacing device as claimed in claim 15, wherein said modification means comprises switch means responsive to said output from said comparator means for enabling access by said processing unit to data in said read-only memory.

19. An interfacing device as claimed in claim 18, wherein said switch means comprises a semiconductor device.

20. An interfacing device as claimed in any one of claims 1 to 19, further comprising case means containing said recognition means and said modification means, said case means including a handle portion.

21. An interfacing device as claimed in claim 20, said external data storage medium being connectable thereto in such a manner as to be positioned underneath said handle portion, and said handle portion being formed with a thumb rest protruding from an upper portion thereof said thumb rest being formed with a concave portion for accommodating the thumb of a user, whereby an assembly of said interfacing device and said external data storage medium can conveniently be grasped with a thumb engaging said thumb rest and fingers engaging said external data storage medium for connection of said assembly to said processing unit of said computer games system.

22. An interfacing device as claimed in claim 21, wherein the protruding thumb rest prevents connection of said assembly to said processing unit in an upside-down relation.

23. An interfacing device as claimed in claim 21, wherein the recognition means and the modification means are incorporated in a printed circuit board that has sufficient thickness that said connection of said assembly to said processing unit of said computer games system can be effected with movement that is rectilinear.

24. An interfacing device according to claim 1 that operates in a latch-setting mode wherein a user can predetermine said selected address and a characteristic of said modification of data and in an active mode wherein said recognition means recognize said selected address and said modification means effects said modification of data in response to said recognition.

25. An interfacing device according to claim 24, further comprising a display screen comprising a plurality of character cells each measuring a plurality of pixels in each of two mutually orthogonal directions.

26. An interfacing device according to claim 25, wherein at least in the latch-setting mode, a plurality of pixels in each cell are controlled as a unit.

27. An interfacing device according to claim 26, wherein at least, in said latch-setting mode, said display screen presents a graphic display and further comprising graphic generating means for generating said graphic display.

28. An interfacing device according to claim 27, wherein said graphic generating means comprises a plurality of gate means responsive to graphic address signals and a graphic output buffer responsive to said gate means and producing graphic data outputs that control said pixels, whereby said graphics display is generated without the provision of a read-only memory.

29. A computer games system comprising a processing unit, an external data storage medium, and an interfacing device as claimed in any one of claims 1 to 28 for interconnecting the processing unit and the external data storage medium.

30. A method of playing a computer game using a computer games system having a processing unit and an external data storage medium, comprising the steps of comparing an address from the processing unit with a selected address and modifying data processed by the processing unit whenever the compared addresses are the same.

31. A method as claimed in claim 30, wherein said address is either selected by a player of the game or is presettable.

32. A method as claimed in claim 30 or claim 31, wherein the modification of data processed by the processing unit comprises the step of modifying data supplied to the processing unit from the external data storage medium.

33. A method as claimed in claim 30 or claim 31, wherein the processing unit includes an internal memory and the modification of data processed by the processing unit comprises the step of supplying to said processing unit data from a source external to both the external data storage medium and the processing unit in order to modify said internal memory.

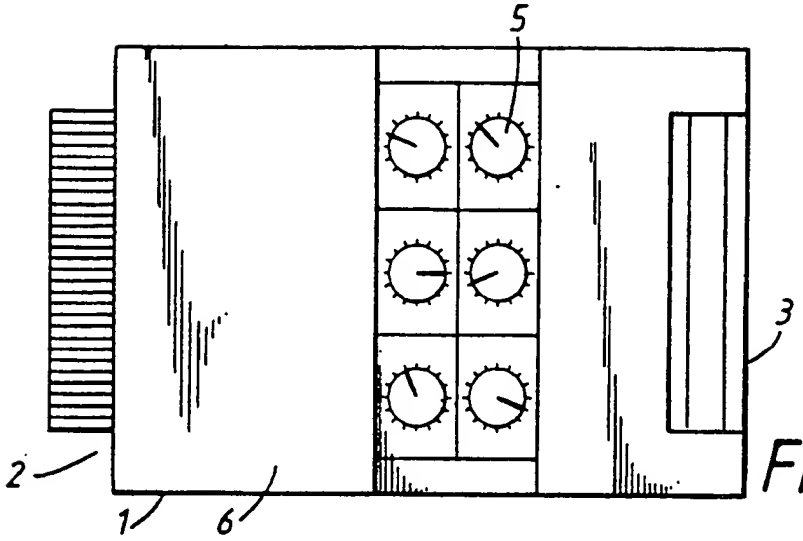

Fig.1(a).

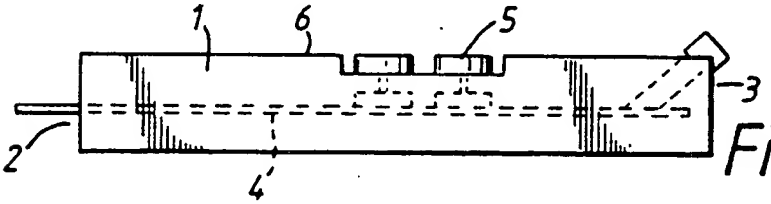

Fig.1(b).

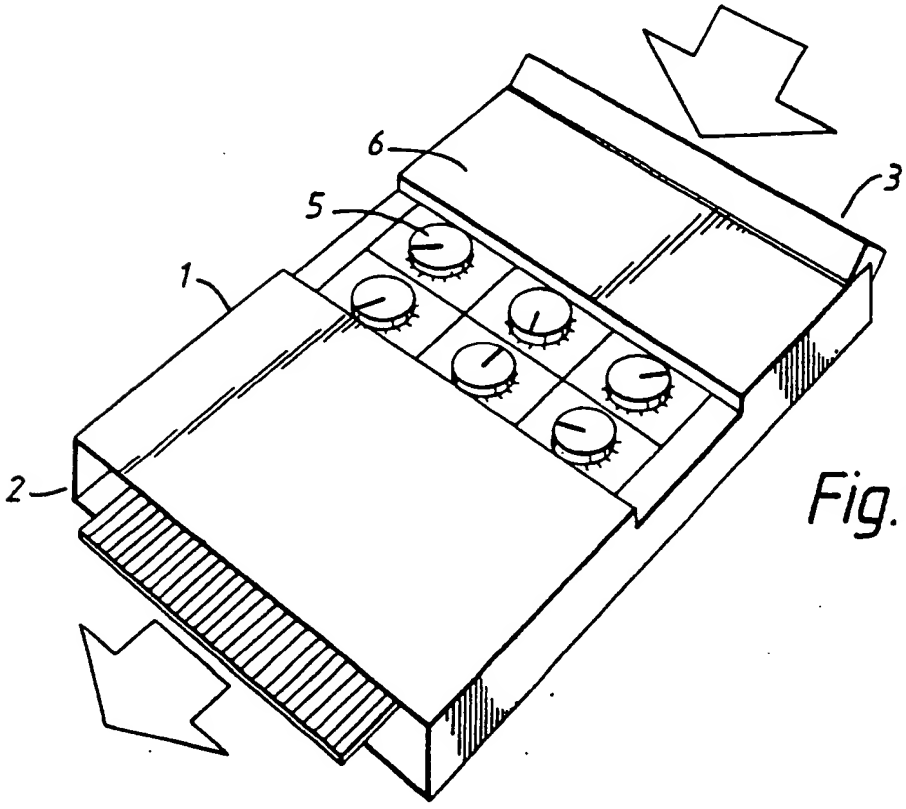

Fig.1(c).

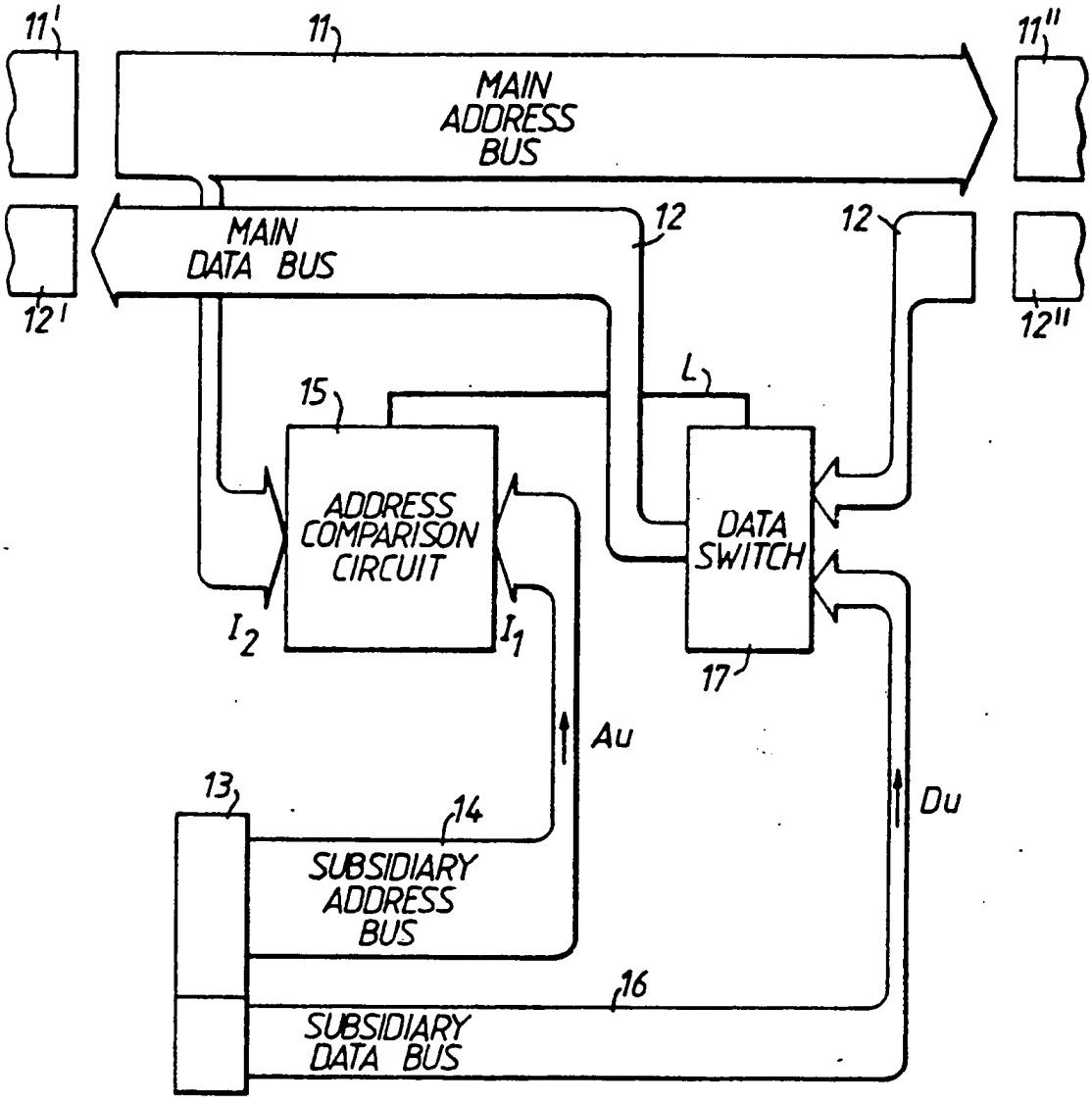
11'
11
11''
MAIN
ADDRESS
BUS
MAIN
DATA BUS
12
12
12'
12''
L
15
ADDRESS
COMPARISON
CIRCUIT
DATA
SWITCH
I2
I1
17
Au
13
14
Du
SUBSIDIARY
ADDRESS
BUS
16
SUBSIDIARY
DATA BUS

Fig.2.

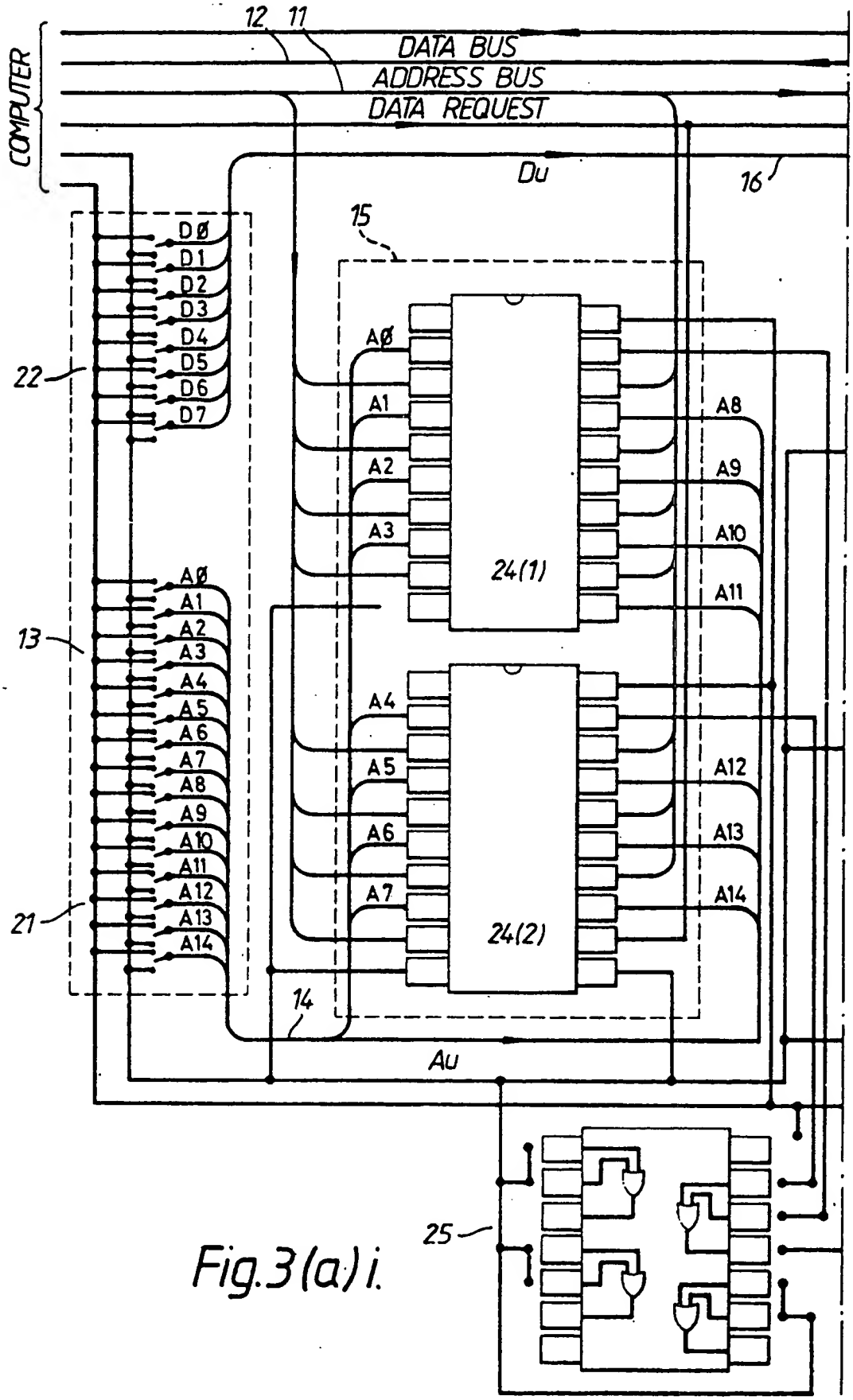
COMPUTER
12
11
DATA BUS
ADDRESS BUS
DATA REQUEST
Du
16
15
22
D0
D1
D2
D3
D4
D5
D6
D7
A0
A1
A2
A3
24(1)
A8
A9
A10
A11
13
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
21
A4
A5
A6
A7
24(2)
A12
A13
A14
14
Au
25

Fig.3(a) i.

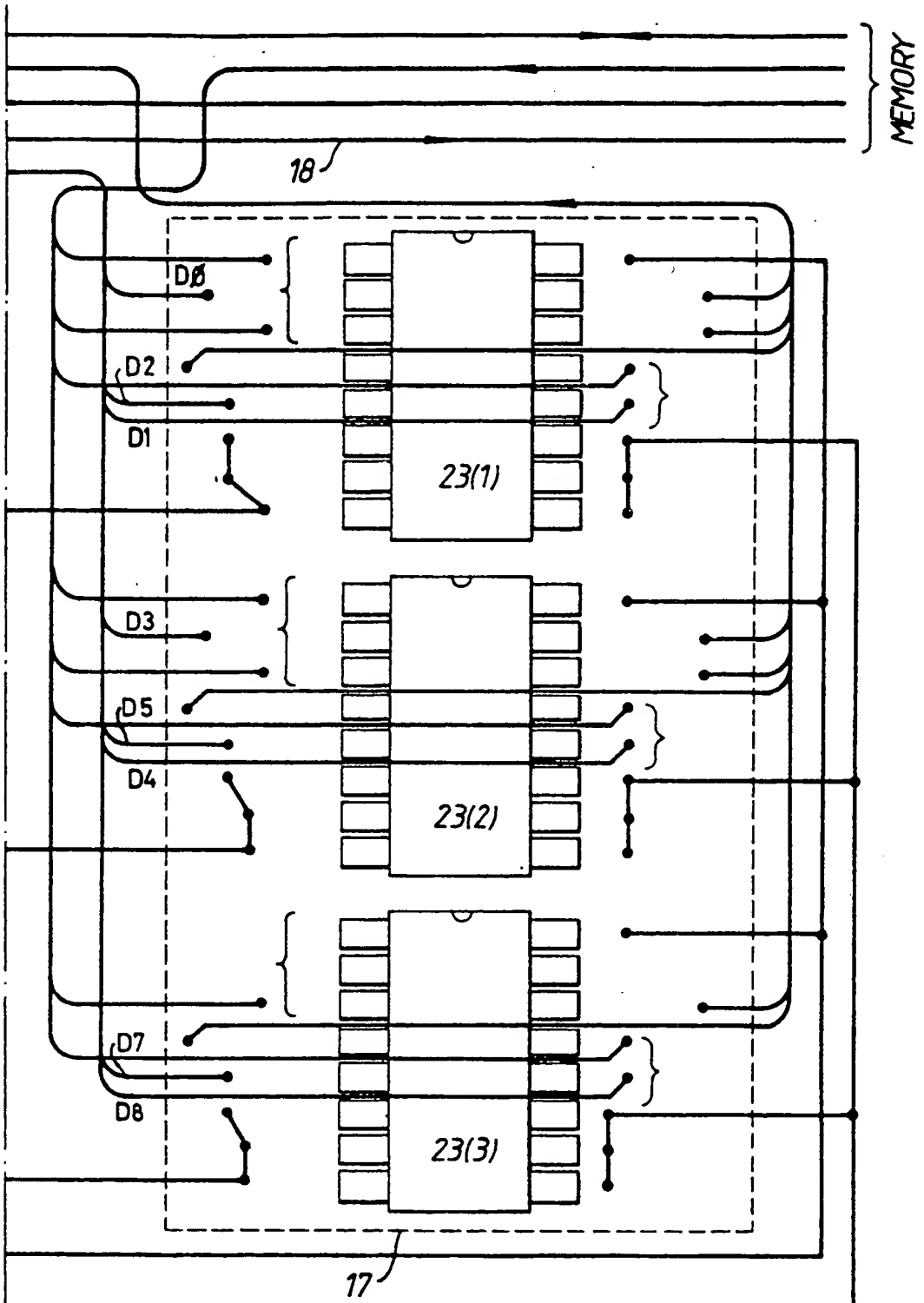

Fig.3(a) ii.

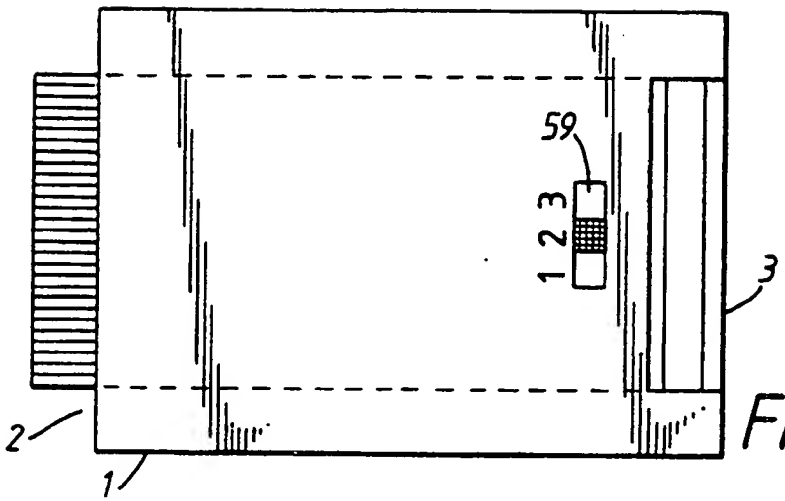

Fig.4(a).

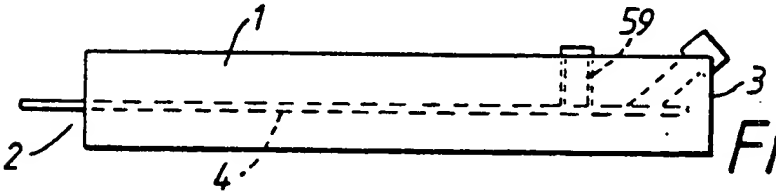

Fig.4(b).

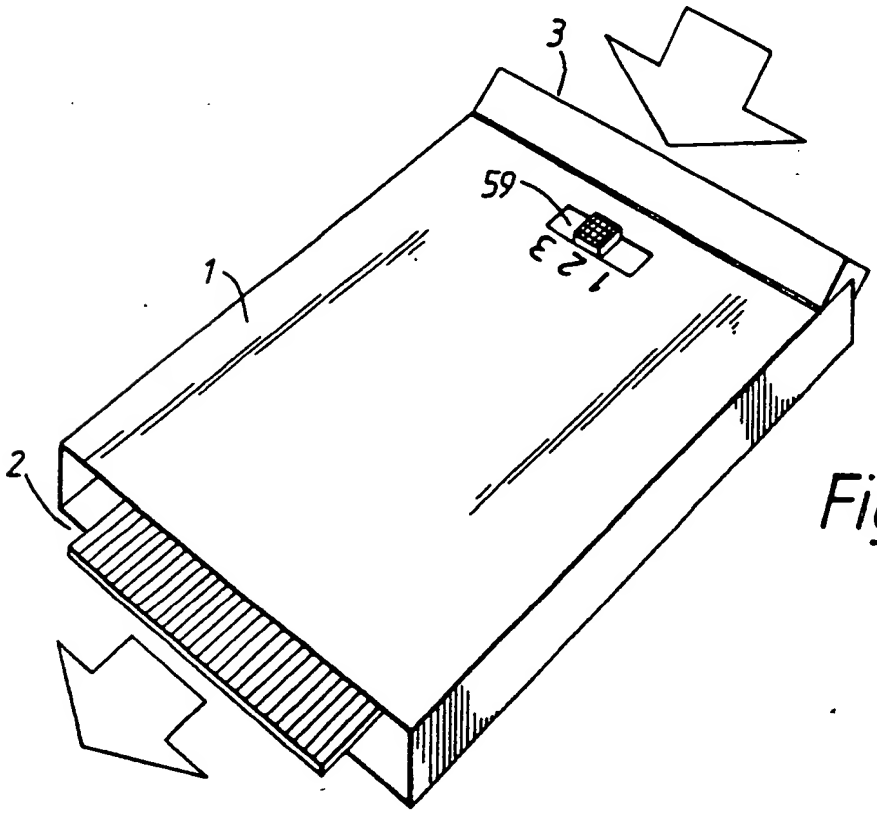

Fig.4(c).

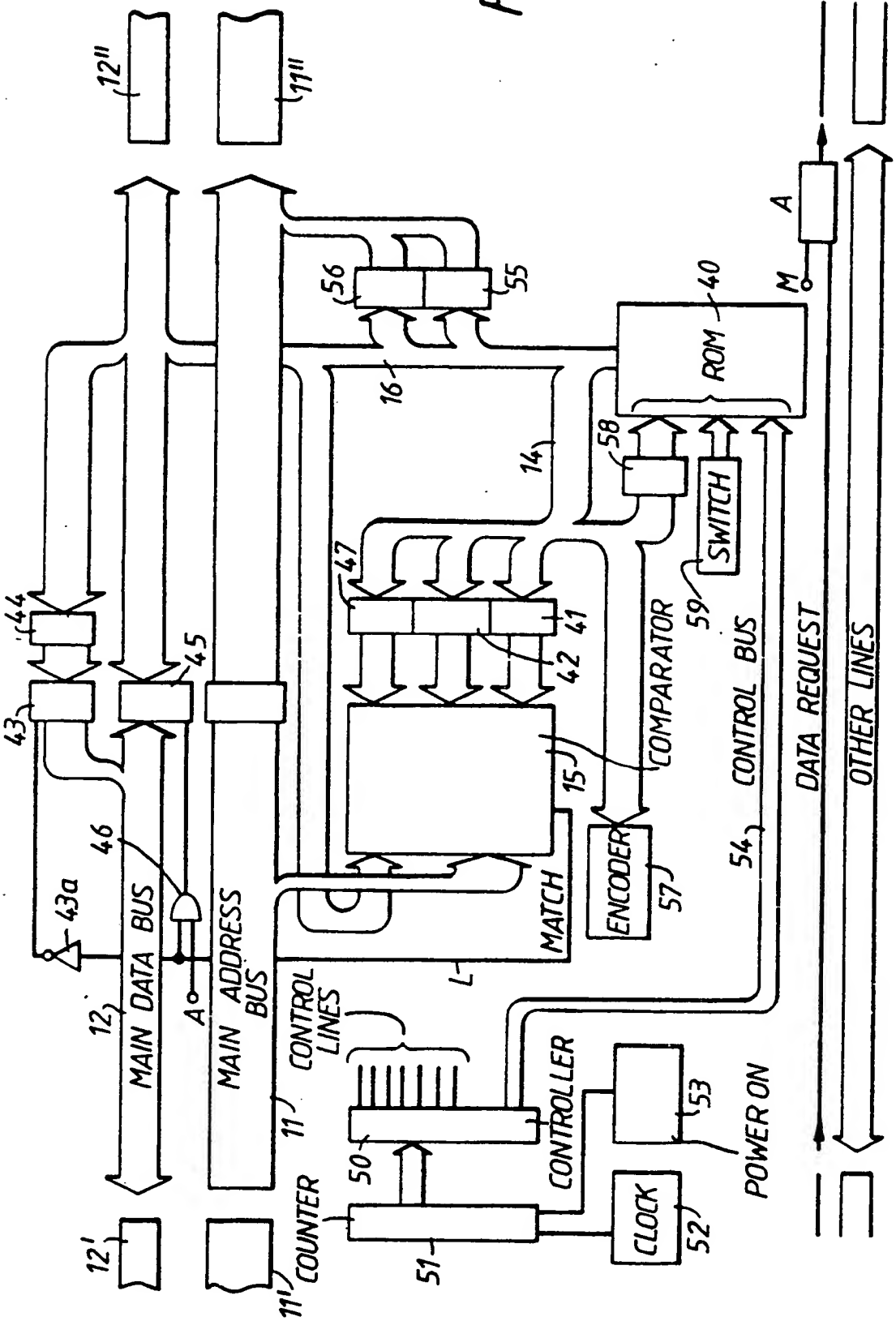
12''
11''
56
55
16
14
58
ROM
40
M
A
SWITCH
59
47
41
42
44
45
43
COMPARATOR
CONTROL BUS
DATA REQUEST
OTHER LINES
46
43a
MAIN DATA BUS
MAIN ADDRESS BUS
MATCH
15
ENCODER
57
54
12
A
L
CONTROL LINES
11
CONTROLLER
53
POWER ON
50
CLOCK
52
12'
11'
COUNTER
51

Fig.5.

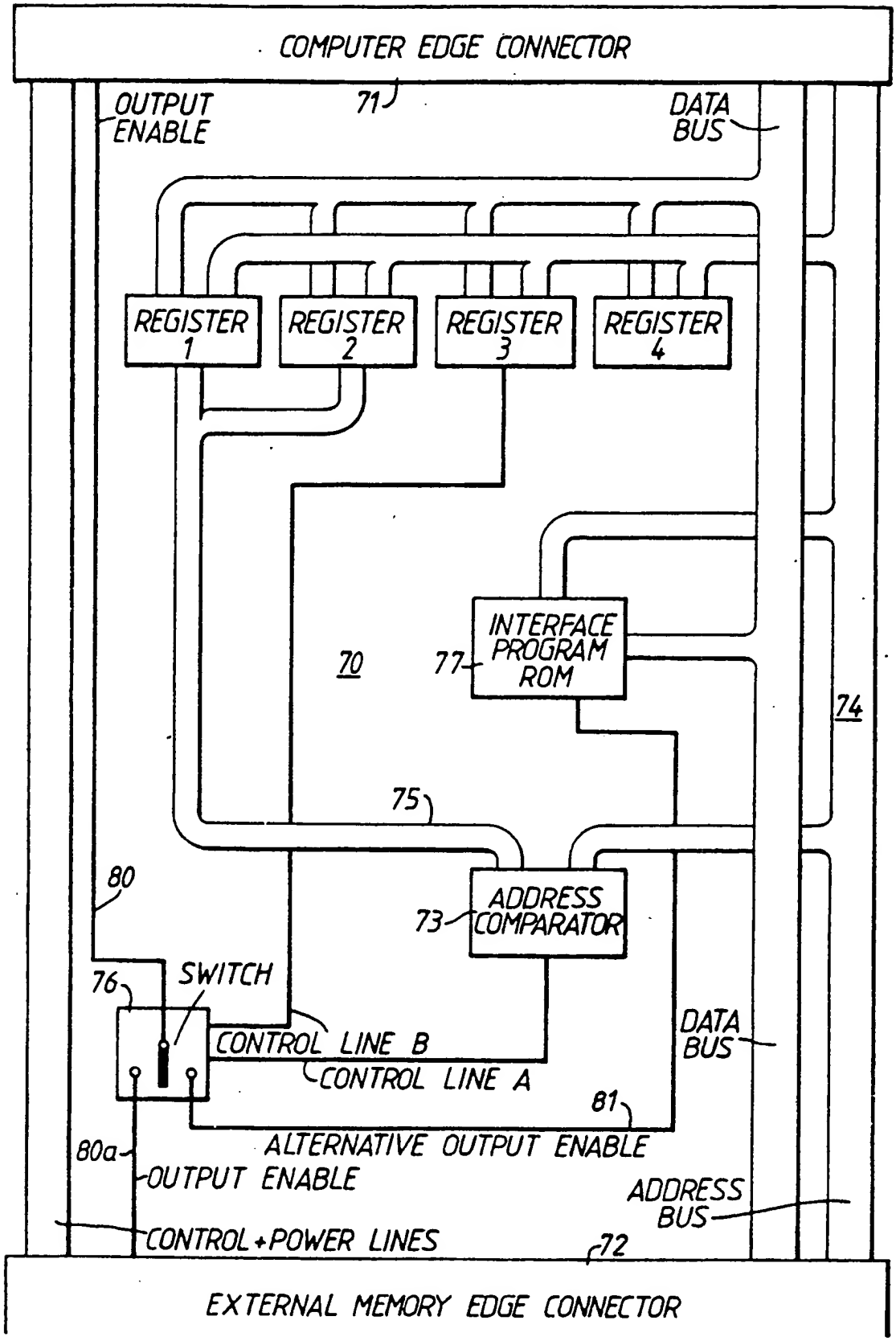
COMPUTER EDGE CONNECTOR
OUTPUT ENABLE
71
DATA BUS
REGISTER 1
REGISTER 2
REGISTER 3
REGISTER 4
INTERFACE PROGRAM ROM
70
77
74
75
80
ADDRESS COMPARATOR
73
SWITCH
76
CONTROL LINE B
CONTROL LINE A
DATA BUS
81
ALTERNATIVE OUTPUT ENABLE
80a
OUTPUT ENABLE
ADDRESS BUS
CONTROL + POWER LINES
72
EXTERNAL MEMORY EDGE CONNECTOR

Fig.6.

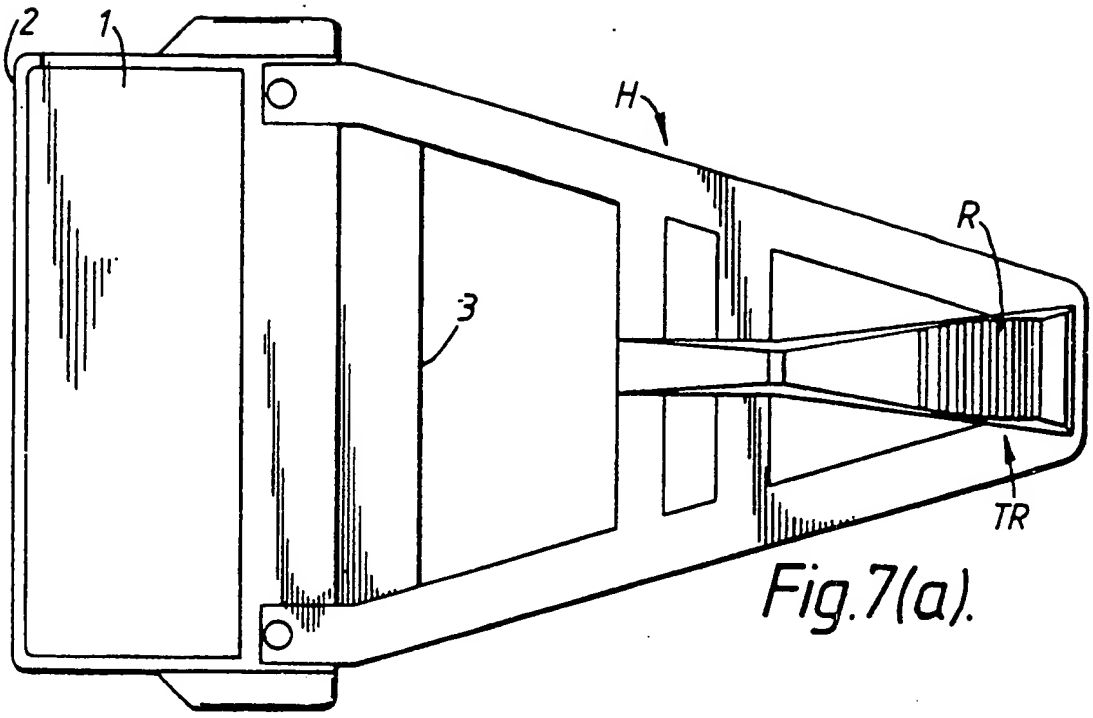

Fig.7(a).

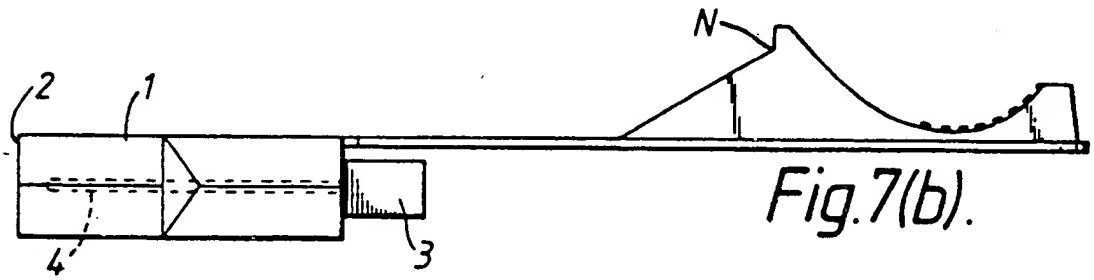

Fig.7(b).

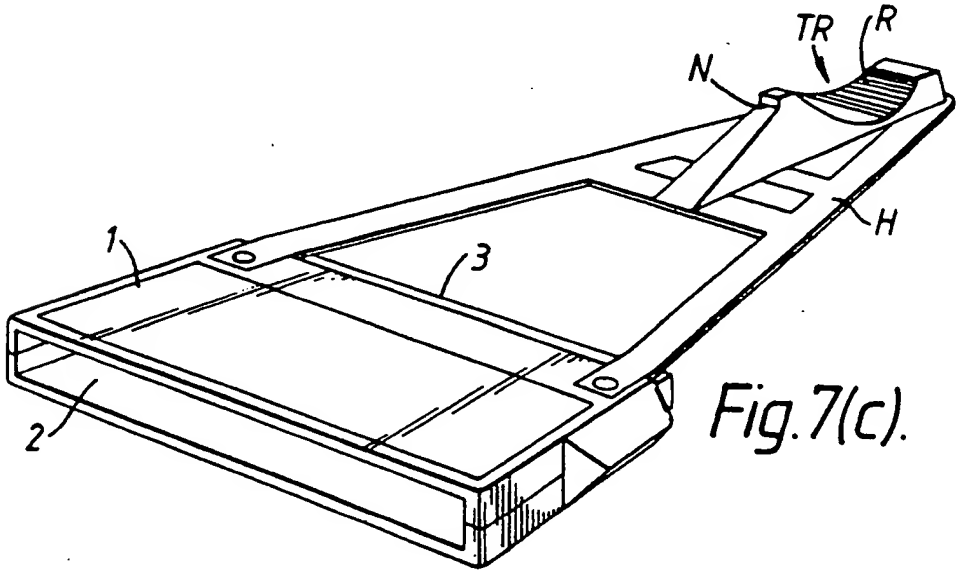

Fig.7(c).

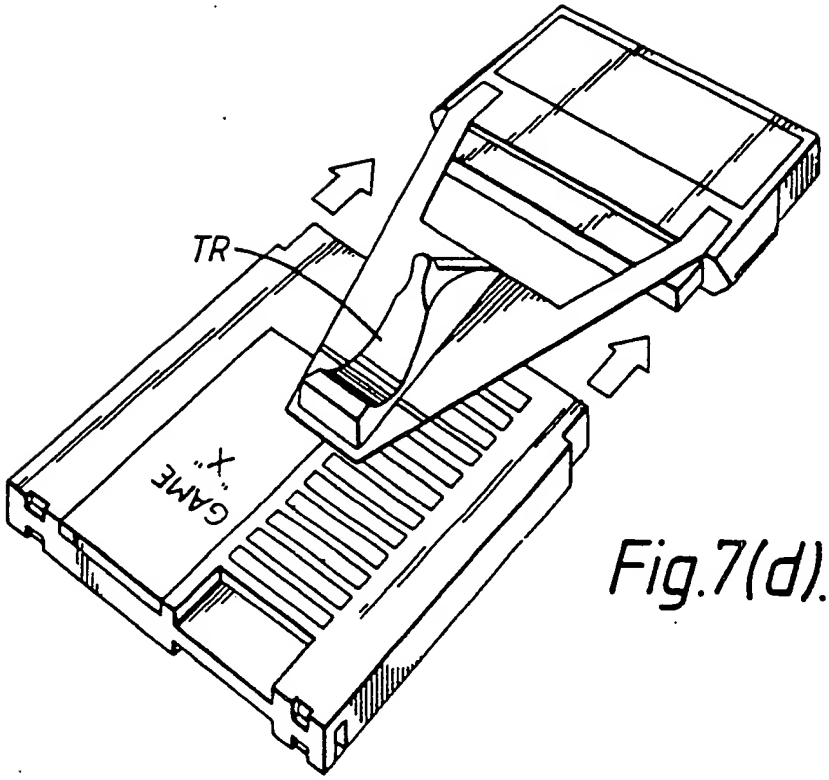

Fig.7(d).

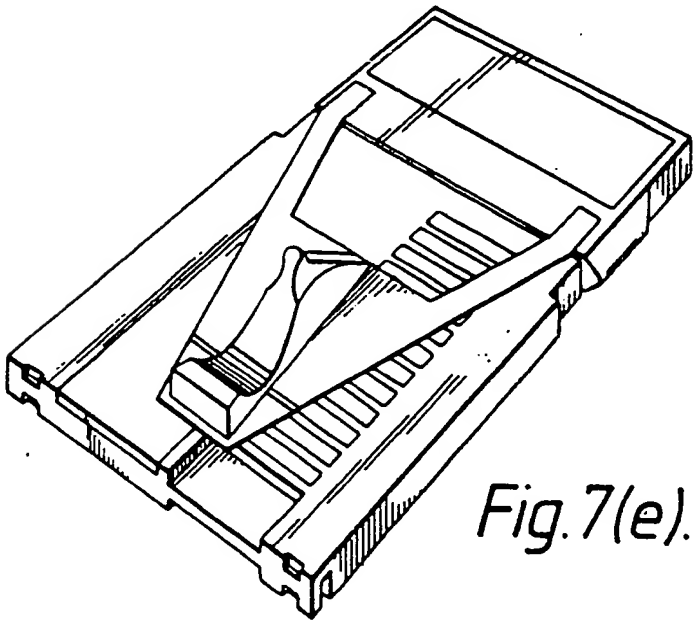

Fig.7(e).

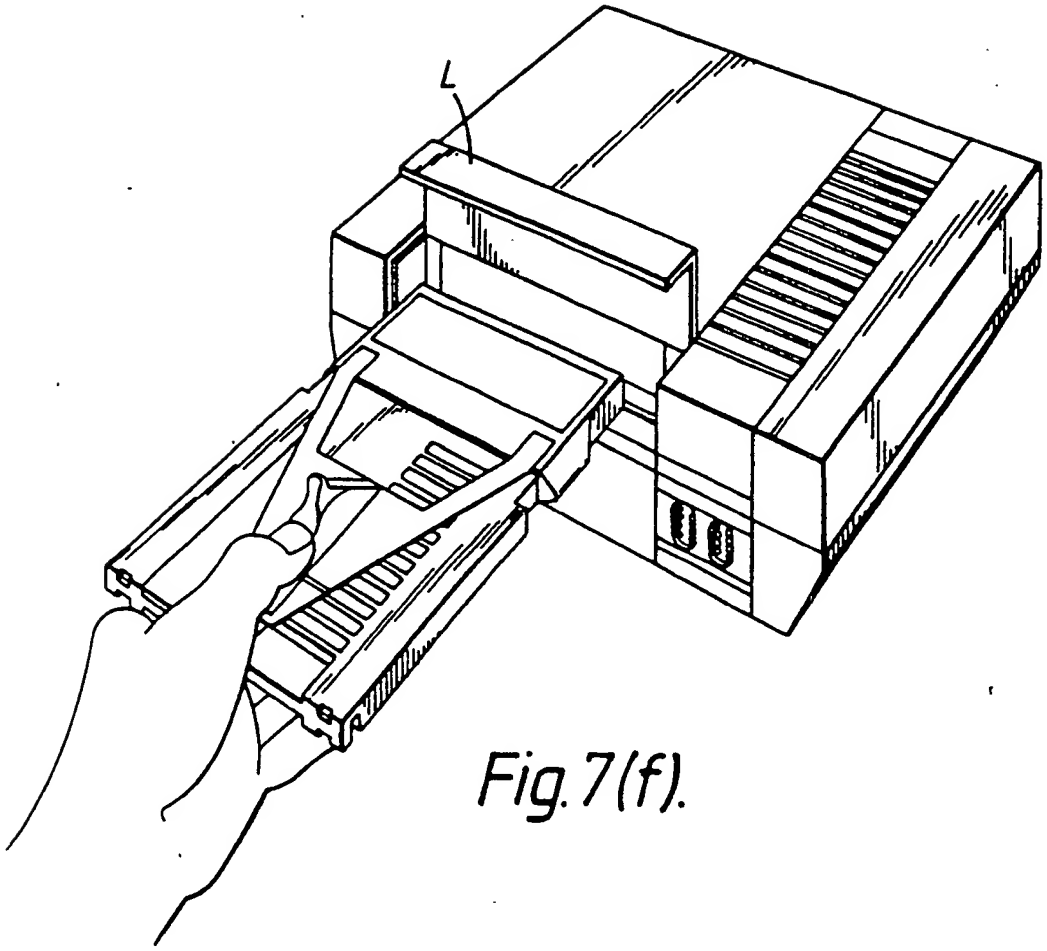

Fig. 7(f).

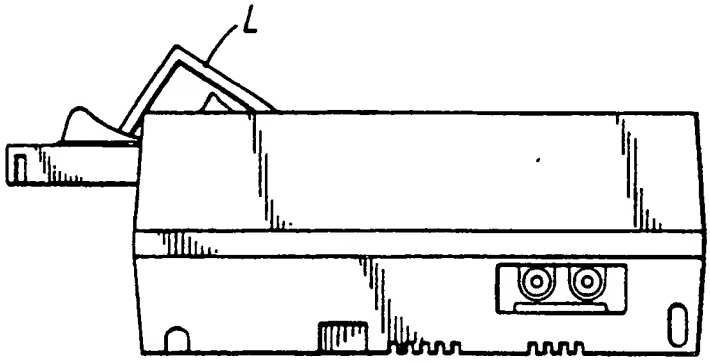

Fig. 7(g).

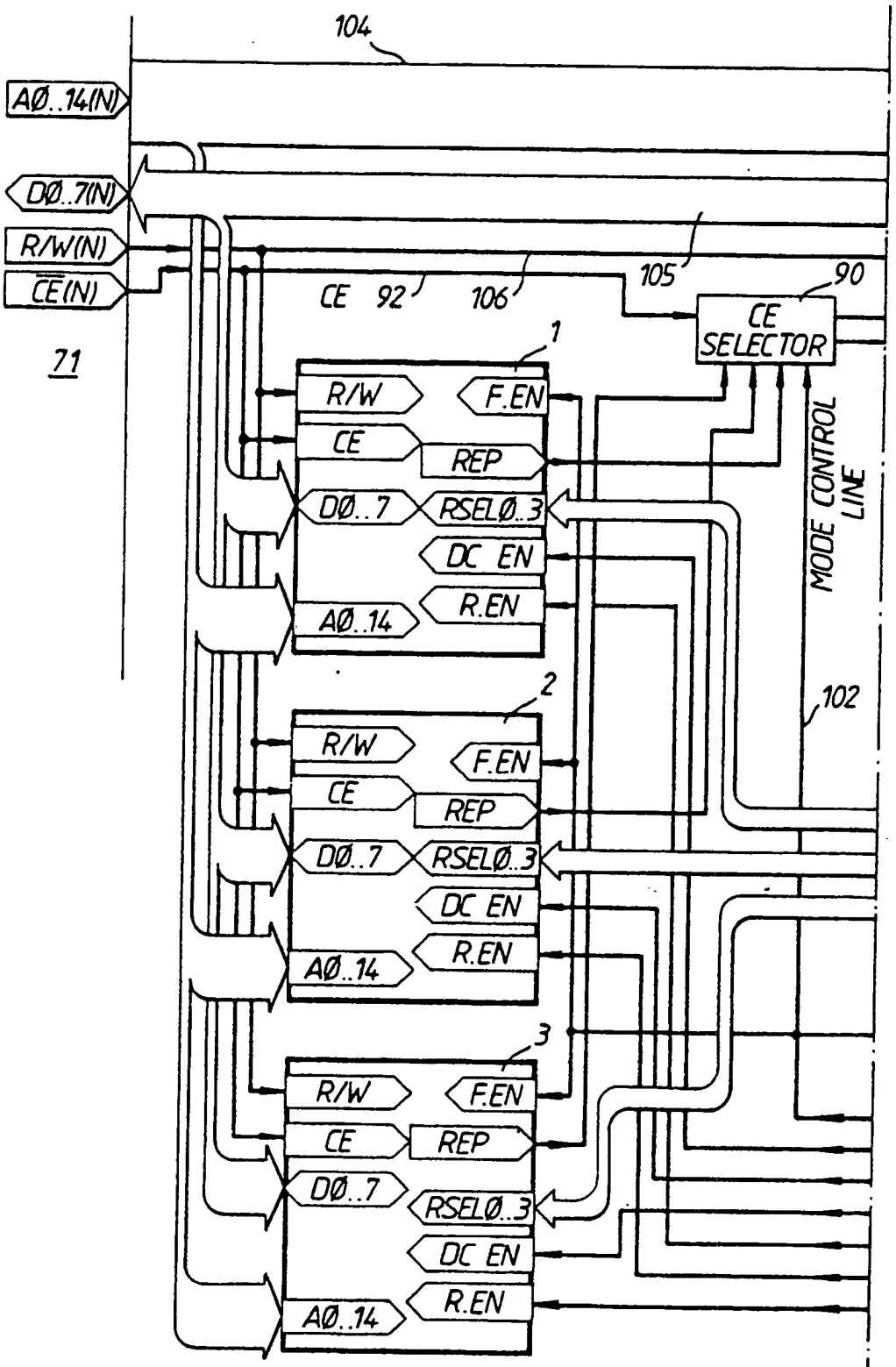
104
A0..14(N)
D0..7(N)
R/W(N)
CE(N)
71
CE
92
106
105
90
CE SELECTOR
1
R/W
F.EN
CE
REP
D0..7
RSEL0..3
DC EN
R.EN
A0..14
MODE CONTROL LINE
102
2
3

Fig.8(a) i.

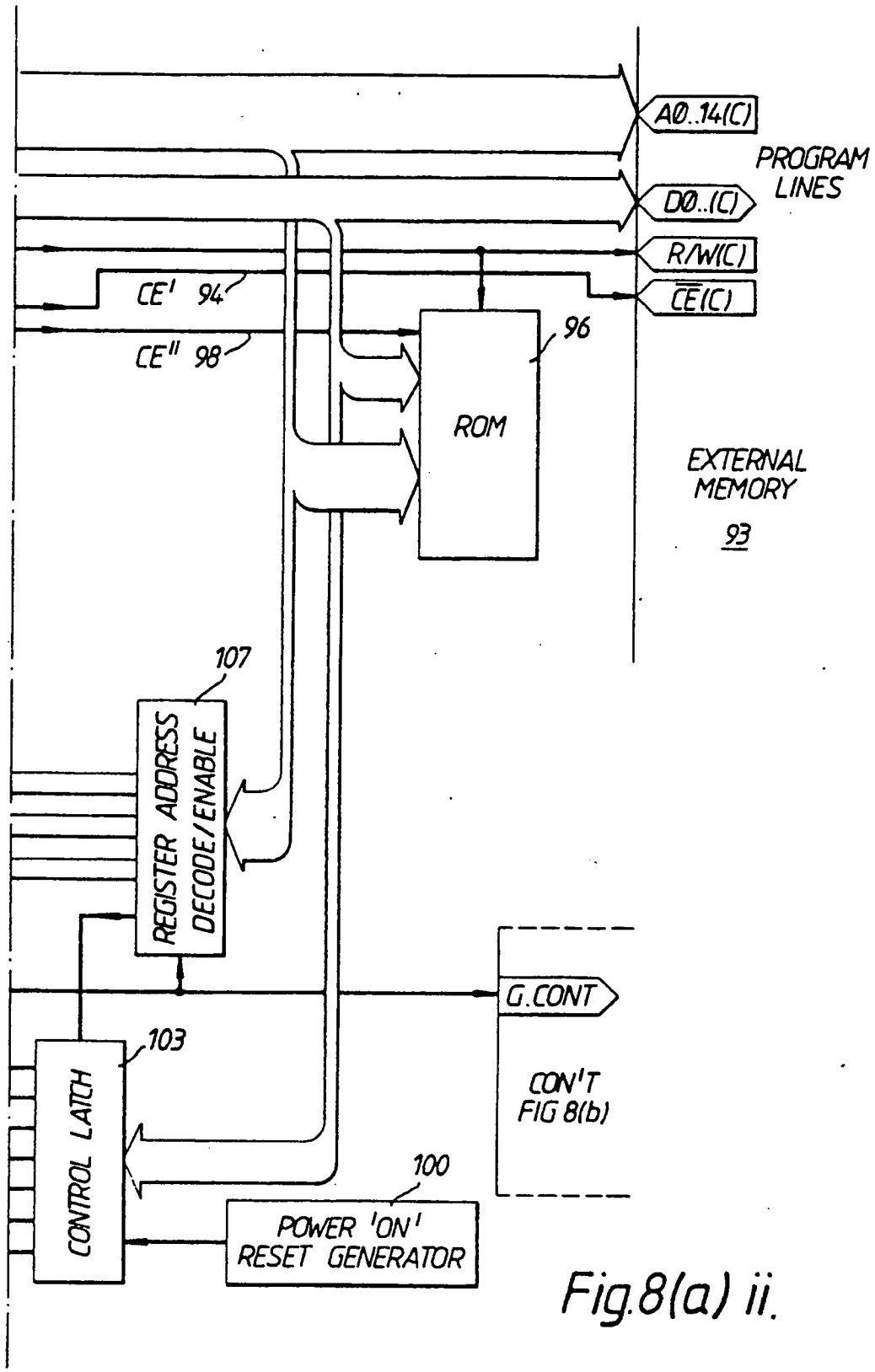
A0..14(C)
PROGRAM LINES
D0..(C)
R/W(C)
CE(C)
CE' 94
CE'' 98
96
ROM
EXTERNAL MEMORY
93
107
REGISTER ADDRESS DECODE/ENABLE
G.CONT
CON'T FIG 8(b)
103
CONTROL LATCH
100
POWER 'ON' RESET GENERATOR

Fig.8(a) ii.

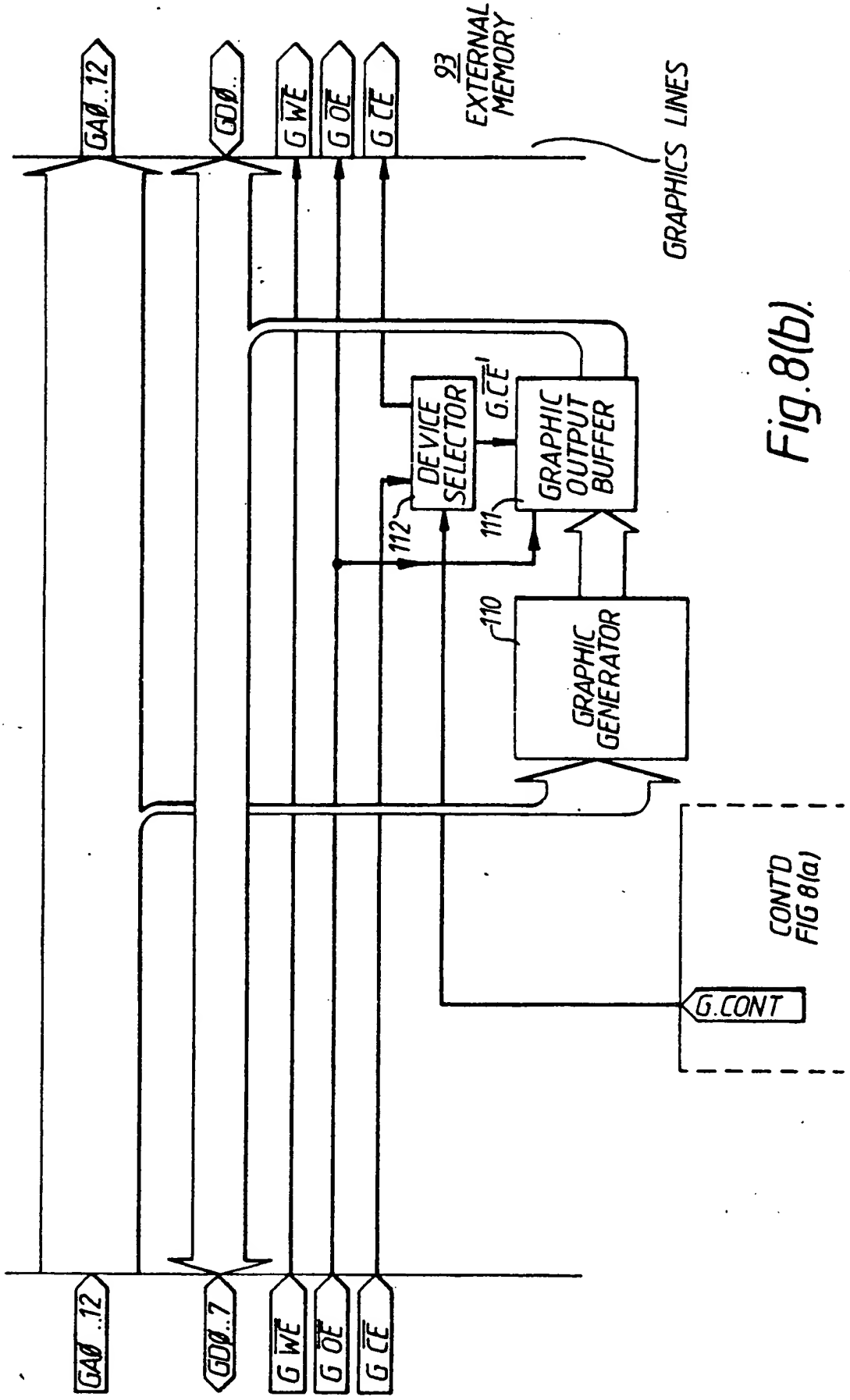
GAØ..12
GDØ..
G WE
G OE
G CE
93
EXTERNAL MEMORY
GRAPHICS LINES
DEVICE SELECTOR
G.CE'
GRAPHIC OUTPUT BUFFER
112
111
110
GRAPHIC GENERATOR
CONT'D FIG 8(a)
G.CONT
GAØ..12
GDØ..7
G WE
G OE
G CE

Fig.8(b).

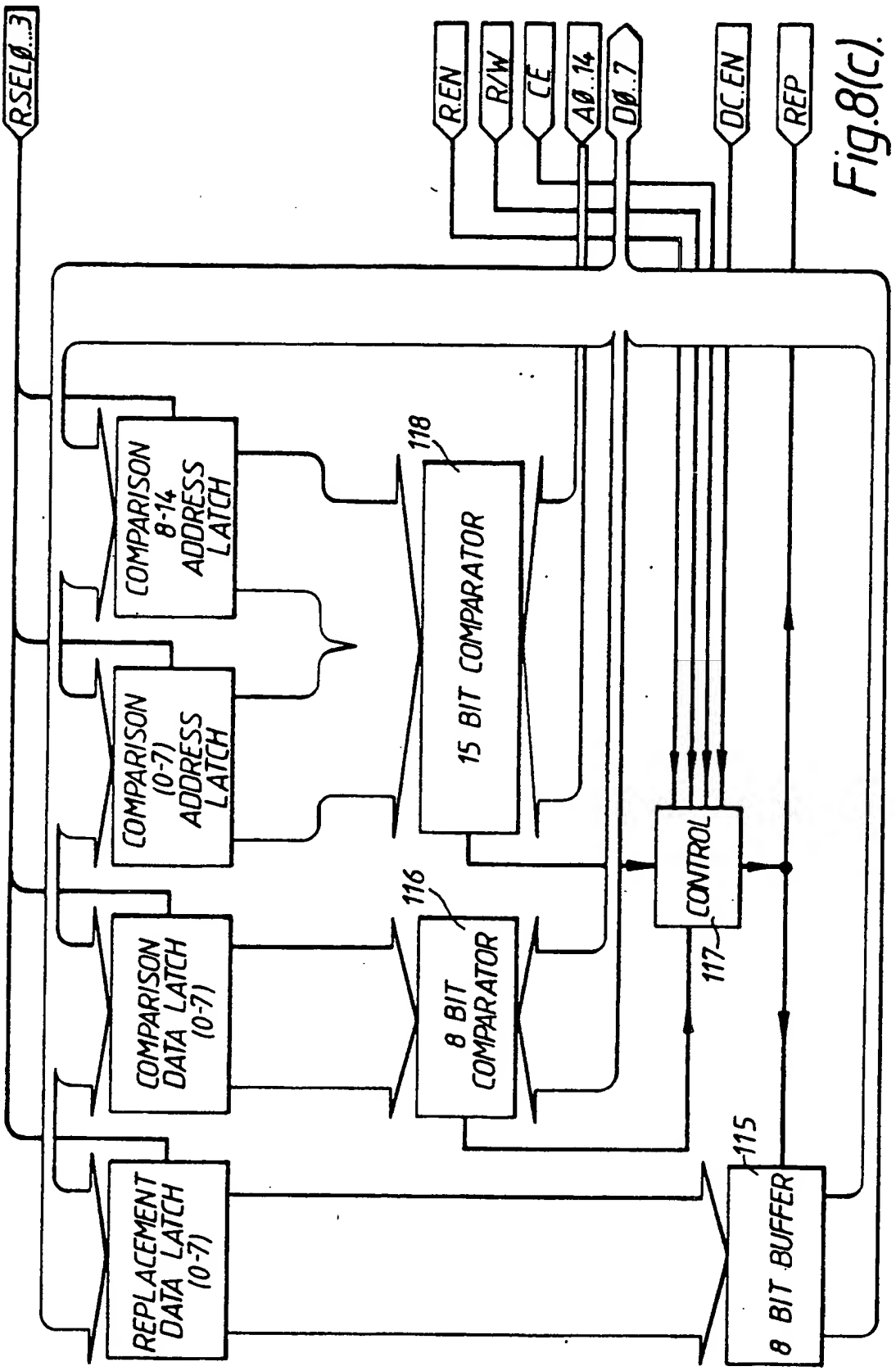
RSELØ...3
R.EN
R/W
CE
AØ..14
DØ..7
OC.EN
REP
COMPARISON 8-14 ADDRESS LATCH
COMPARISON (0-7) ADDRESS LATCH
COMPARISON DATA LATCH (0-7)
REPLACEMENT DATA LATCH (0-7)
118
15 BIT COMPARATOR
116
8 BIT COMPARATOR
CONTROL
117
115
8 BIT BUFFER

Fig.8(c).

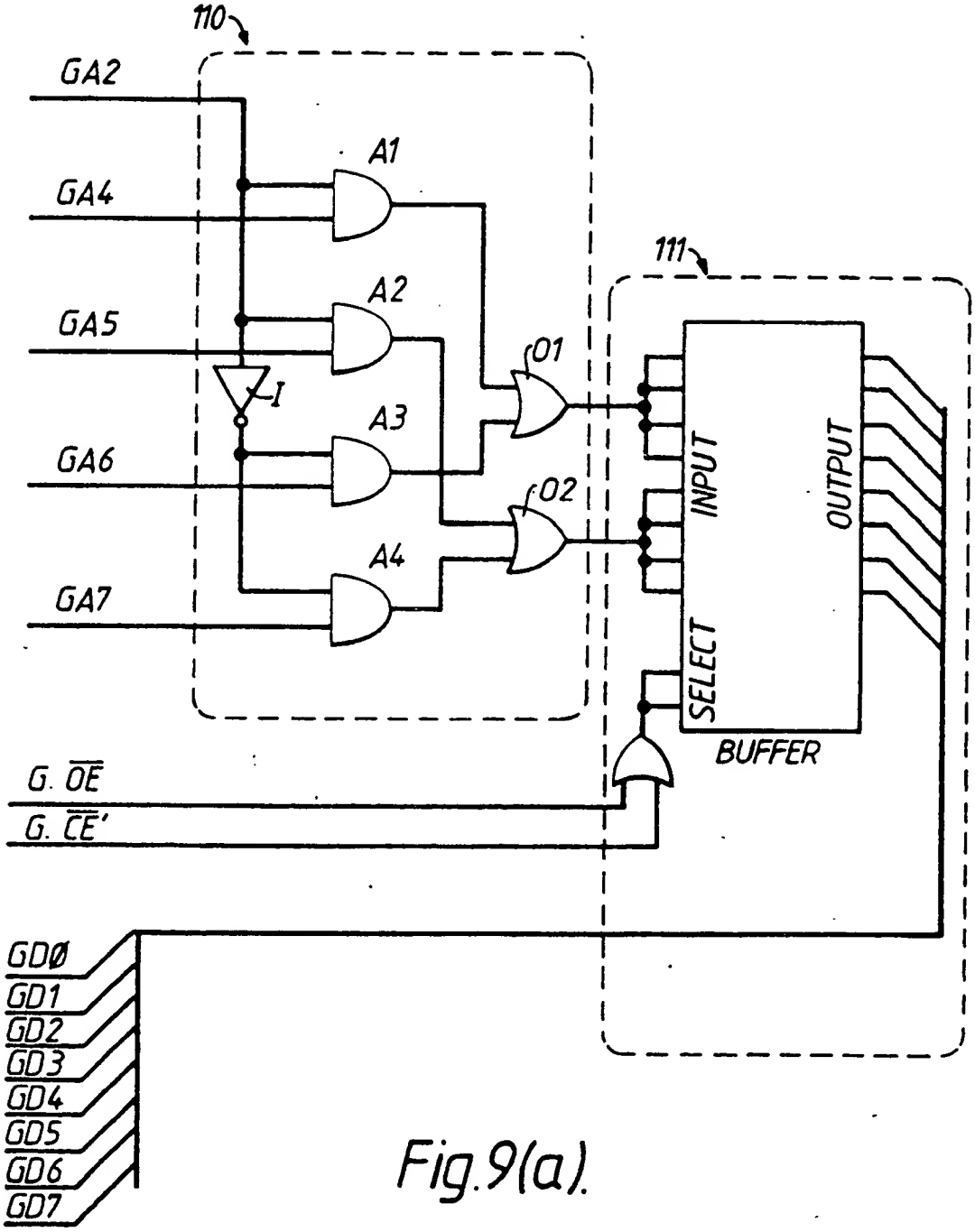
110
GA2
GA4
GA5
GA6
GA7
A1
A2
A3
A4
I
O1
O2
111
INPUT
OUTPUT
SELECT
BUFFER
G. $\overline{OE}$
G. $\overline{CE}$'
GDØ
GD1
GD2
GD3
GD4
GD5
GD6
GD7

Fig.9(a).

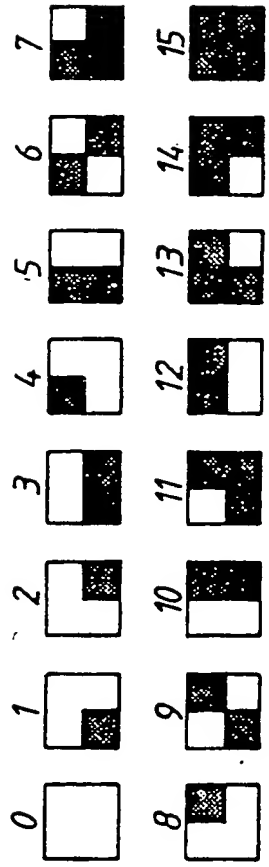
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15

Fig.9(b)

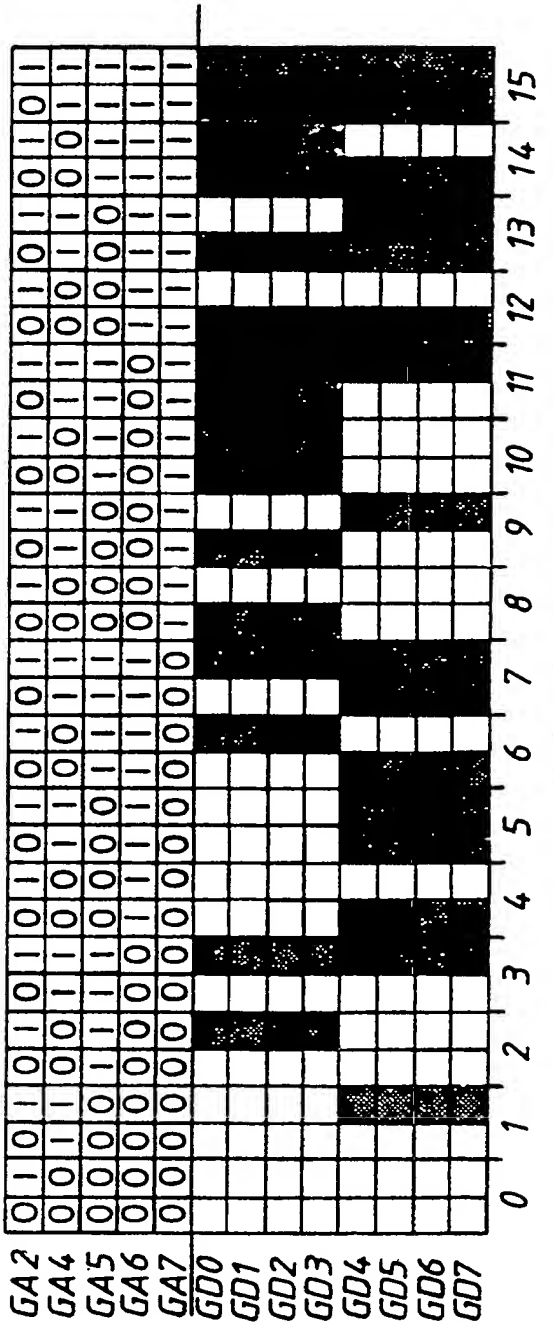
GA2
GA4
GA5
GA6
GA7
GD0
GD1
GD2
GD3
GD4
GD5
GD6
GD7
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
CHARACTER CELLS

Fig.9(c)

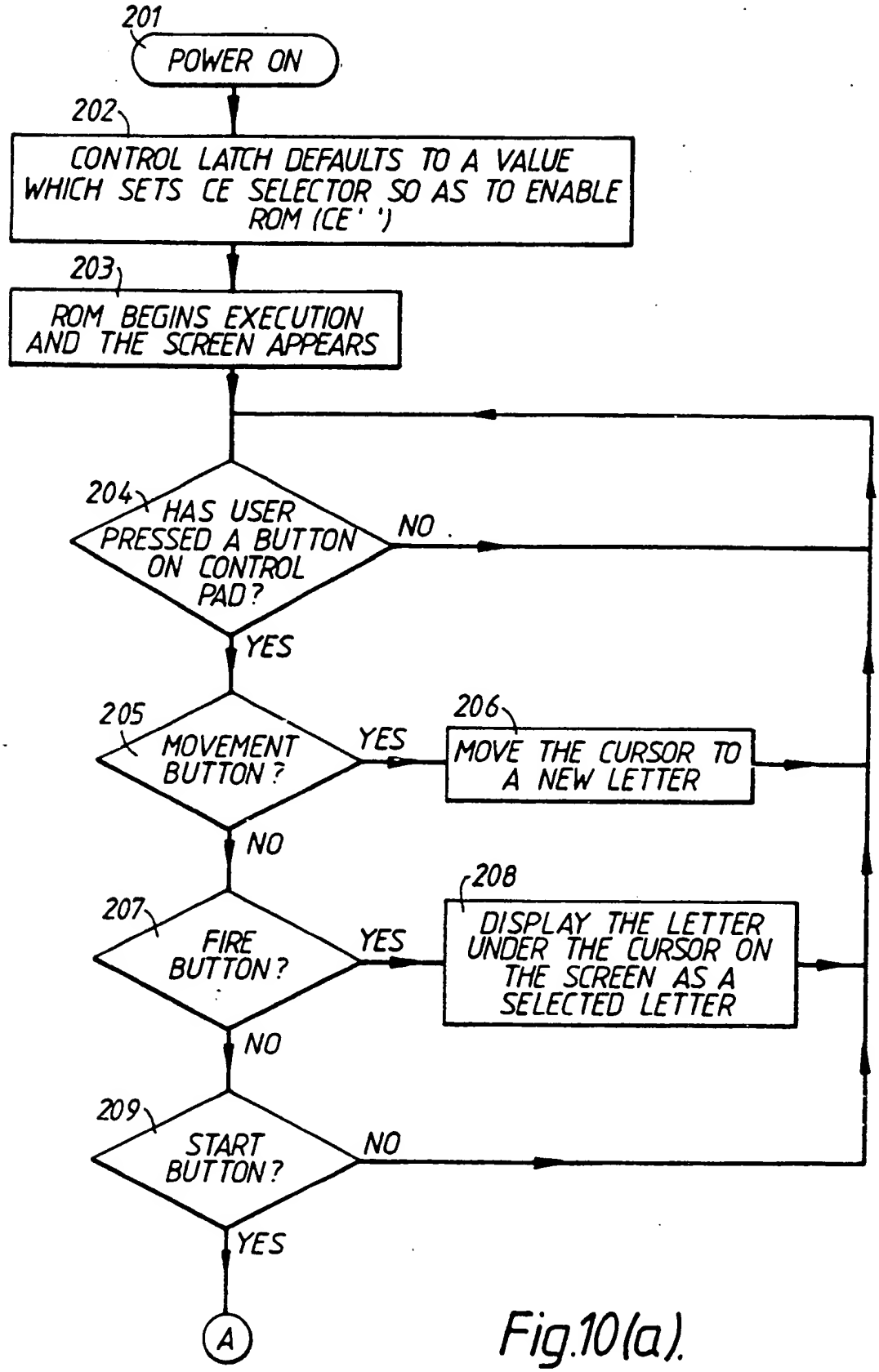
201
POWER ON
202
CONTROL LATCH DEFAULTS TO A VALUE WHICH SETS CE SELECTOR SO AS TO ENABLE ROM (CE' ')
203
ROM BEGINS EXECUTION AND THE SCREEN APPEARS
204
HAS USER PRESSED A BUTTON ON CONTROL PAD?
NO
YES
205
MOVEMENT BUTTON?
YES
206
MOVE THE CURSOR TO A NEW LETTER
NO
207
FIRE BUTTON?
YES
208
DISPLAY THE LETTER UNDER THE CURSOR ON THE SCREEN AS A SELECTED LETTER
NO
209
START BUTTON?
NO
YES
A

Fig.10(a).

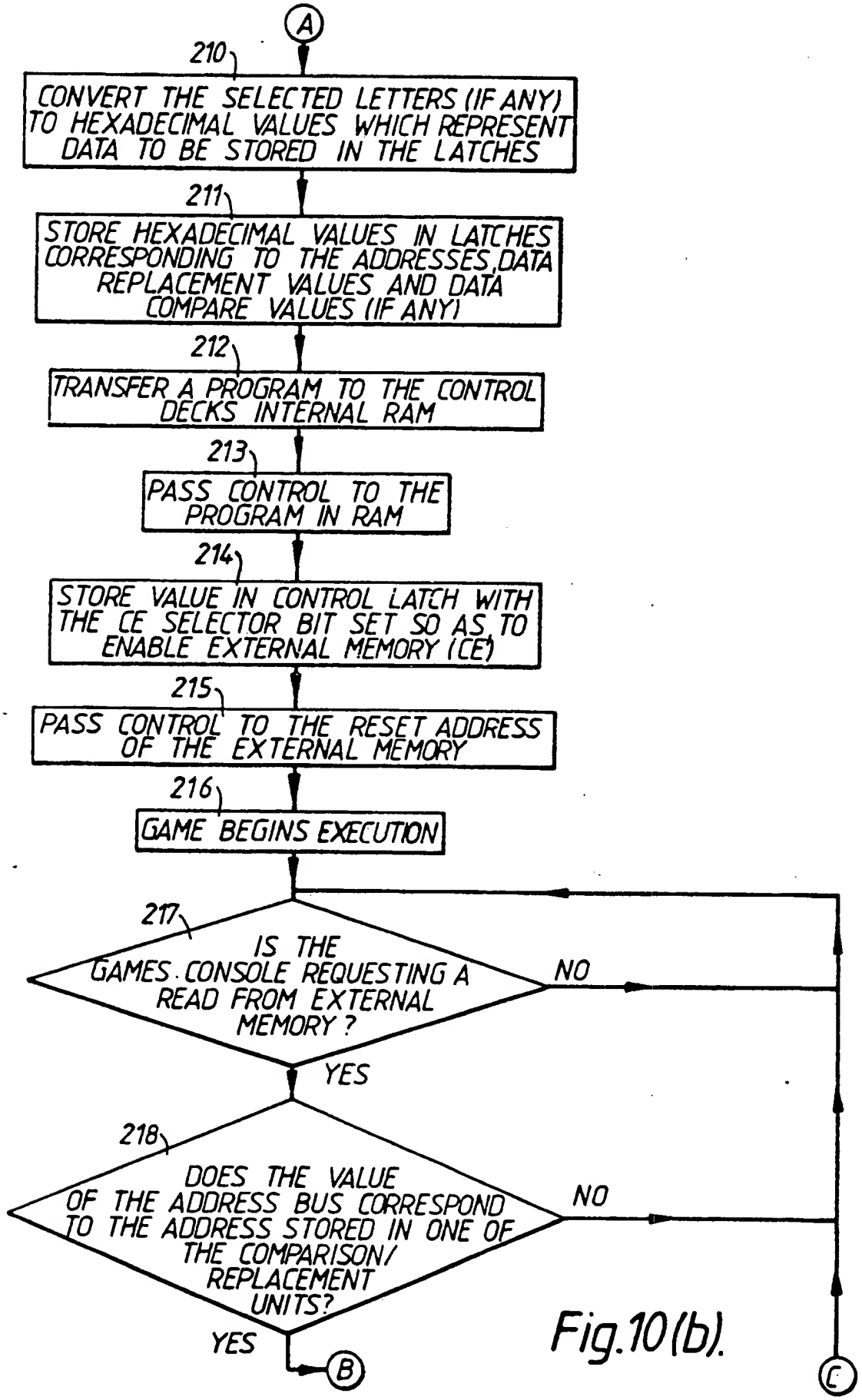
A
210
CONVERT THE SELECTED LETTERS (IF ANY) TO HEXADECIMAL VALUES WHICH REPRESENT DATA TO BE STORED IN THE LATCHES
211
STORE HEXADECIMAL VALUES IN LATCHES CORRESPONDING TO THE ADDRESSES, DATA REPLACEMENT VALUES AND DATA COMPARE VALUES (IF ANY)
212
TRANSFER A PROGRAM TO THE CONTROL DECKS INTERNAL RAM
213
PASS CONTROL TO THE PROGRAM IN RAM
214
STORE VALUE IN CONTROL LATCH WITH THE CE SELECTOR BIT SET SO AS TO ENABLE EXTERNAL MEMORY (CE)
215
PASS CONTROL TO THE RESET ADDRESS OF THE EXTERNAL MEMORY
216
GAME BEGINS EXECUTION
217
IS THE GAMES CONSOLE REQUESTING A READ FROM EXTERNAL MEMORY ?
NO
YES
218
DOES THE VALUE OF THE ADDRESS BUS CORRESPOND TO THE ADDRESS STORED IN ONE OF THE COMPARISON/ REPLACEMENT UNITS?
NO
YES
B
C

Fig.10(b).

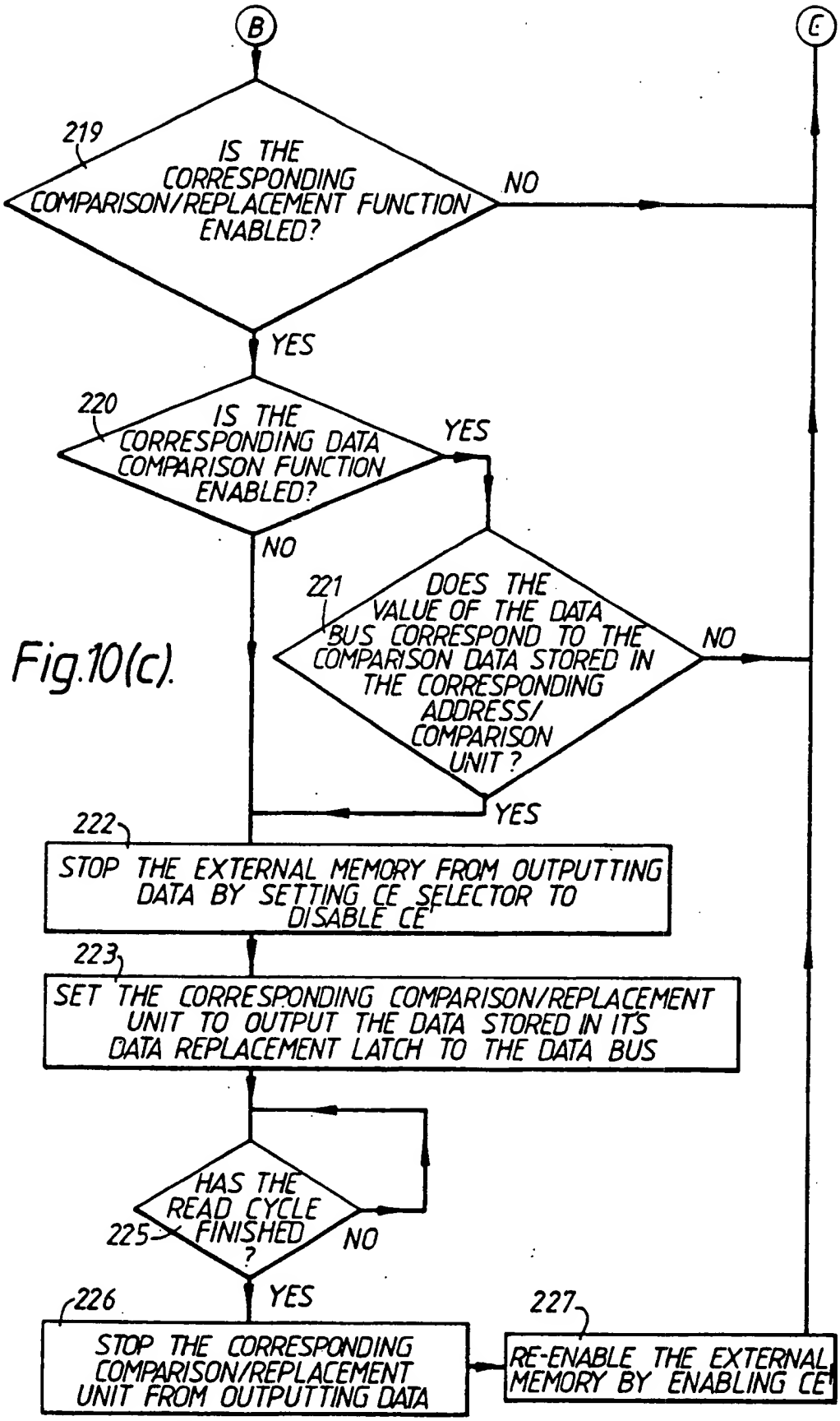
B
C
219
IS THE CORRESPONDING COMPARISON/REPLACEMENT FUNCTION ENABLED?
NO
YES
220
IS THE CORRESPONDING DATA COMPARISON FUNCTION ENABLED?
YES
NO
221
DOES THE VALUE OF THE DATA BUS CORRESPOND TO THE COMPARISON DATA STORED IN THE CORRESPONDING ADDRESS/ COMPARISON UNIT ?
NO
YES
222
STOP THE EXTERNAL MEMORY FROM OUTPUTTING DATA BY SETTING CE SELECTOR TO DISABLE CE
223
SET THE CORRESPONDING COMPARISON/REPLACEMENT UNIT TO OUTPUT THE DATA STORED IN ITS DATA REPLACEMENT LATCH TO THE DATA BUS
225
HAS THE READ CYCLE FINISHED ?
NO
YES
226
STOP THE CORRESPONDING COMPARISON/REPLACEMENT UNIT FROM OUTPUTTING DATA
227
RE-ENABLE THE EXTERNAL MEMORY BY ENABLING CE

Fig.10(c).

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(54) Interfacing device for a computer games system.

(57) An interfacing device for connecting the processing unit of a computer games system to an external data storage medium has a user-operable selection unit for generating a user-selected address and user-selected data. The user-operable selection unit may comprise user-operable switches or electronic latches that are set by a program in response to selections made by the user by means of a joystick, keypad or any other input device. An address comparison unit compares the user-selected address with the addresses from the processing unit, and a data switching device causes the user-selected data to be substituted for data in the storage medium whenever the compared addresses are the same. Instead of a user-operable selection unit, preselected addresses and preselected data may be stored in a ROM, which in one embodiment changes the way the computer interprets external memory and in another changes the computer's internal memory itself.

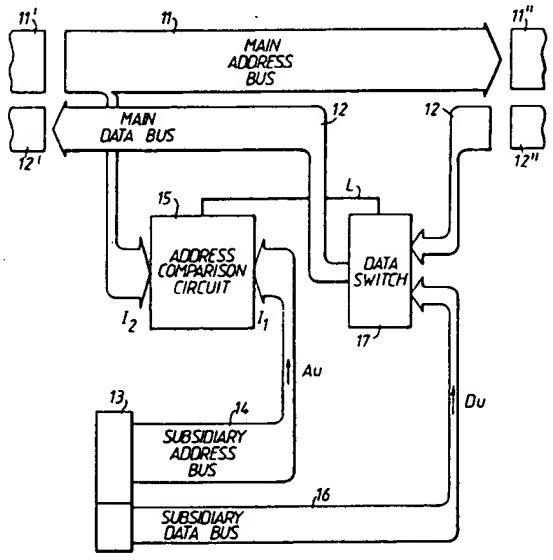

Fig.2.

EP 0 402 067 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 90 30 6034

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	FR-A-2 407 527 (ROCKWELL INTERNATIONAL CORP.) * page 3, line 17 - line 20 * * page 16, line 18 - line 29; claim 3 *	1-6,30-33	G 06 F 15/44
A	EP-A-0 268 419 (NINTENDO CO.LTD.) * abstract *	1-2	
A	GB-A-2 118 809 (ATARI INC.) * abstract; claim 3; figure 2 *	1-6,30-33	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

G 06 F
A 63 F

The present search report has been drawn up for all claims

Place of search	Date of completion of search	Examiner
The Hague	19 February 92	ADMINISTRATION

CATEGORY OF CITED DOCUMENTS

X: particularly relevant if taken alone
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